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Verilog Design of PLL Using Time-To-Digital Converter

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Abstract
The paper Implements The Digital Phase-Locked Loop circuit is implemented in Verilog HDL . Only cells from the standard library were used in its design. The RTL circuit description can be parameterized to enable the construction of circuits with specific properties. The Digital Controlled Oscillator, which is entirely made of NAND components, and a 2-level Time-to-Digital Converter are the foundations of the All Digital Phase-Locked Loop circuit that is being demonstrated. . The most versatile application of PLL is for clock generation and clock recovery in microprocessor and communication systems. Nowadays, due to higher integration of digital designs, digital PLL are preferred. The present work focuses on the design of ADPLL using tool from Xilinx. Code for ADPLL is written in Verilog and compiled using Verilog.
Keywords— digital signal processing; digital phase-locked loop; standard cell library; time-to-digital converter; digital controlled oscillator ; RTL ; Verilog HDL

INTRODUCTION

Nowadays, digital signal processing is essential to communication systems. A high- frequency clock signal is necessary for the precise time control required by digital processing. A crucial component of contemporary digital systems including cellular communications,microcontrollers, and CPUs is the phase-locked loop (PLL). In radio frequency circuits for digital signal processing circuits, it serves as a frequency synthesizer to regulate the frequency or clock data recovery. The law of a very stable low-frequency reference signal is used by PLL to generate a high- frequency clock signal. The digital domain compared to the analog domain provide manifold benefits like easy calibration, higher accuracy, better predictability and the probability to increase the complexity without the need for tedious adjustments or calibrations. Thus the digital domain certainly provides a better edge over analog domain which attracts more research and experimentation in this field of study.

1. LITERATURE SURVEY

Ronald E Best gives an introduction to PLL and deals with theory, design and applications of Mixed PLLs and Digital PLLs. The discussion includes different types of phase detector(linear and digital), phase frequency detectors with charge pump, Loop Filter and VCOs/NCOs .Shabaany, presentsa 0.7-to-1.1-GHz all-digital phase locked loop with a new phase frequency detector and controlled oscillator with body-biasing is presented. Digital-to-voltage converter is controlled the bulk voltage in proposed voltage controlled oscillator, which results high frequency resolution and low power consumption. A search algorithm was used to generates the digital code for the digital-to-voltage converter. This all- digital phase locked loop uses a new structure for thephase-frequency-detector, which ensures high accuracy at phase frequency detecting and increasinglock speed. The proposed design was evaluated in PTM 65nm. The power consumption of the proposedcircuit at 900 MHz frequency is 4.8mW. Kumm,M presents an all-digital phase-locked loop (ADPLL), and it is implemented on a field- programmable gate array. All components like the phase detector (PD), oscillator, and loop filter are realized as digital discrete-time components fed from analog-to-digital converters. The phase detection is realized bygenerating first an analytic signal using a compact implementation of the Hilbert transform and thencomputing the instantaneous phase with the CORDIC algorithm. Das A presents a linear all- digital phase locked loop based on FPGA. In this ADPLL the phase detection system is realized by generating an analytic signal using a compact implementation of Hilbert transform and then simply computing the instantaneous phase using

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CORDIC algorithm in vectoring mode of operation. A 16-bit pipelined CORDIC algorithm is employed in order to obtain the phase information of the signal. Our work is based on Sharma. In this work, a design of an All-Digital Phase Locked Loop (ADPLL) IP core using an accumulator type DCO is proposed in order to generate desired frequency signals. Faster and efficient operation of PLLs was very much desired. Implementation of a digital PLL on a FPGA was used to control the jitter involved in the operation of PLLs to a greater extent that is troubling the current communication industry.

2. PHASE LOCKED LOOP

A phase-locked loop or phase lock loop (PLL) is acontrol system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Phase-locked loop sare widely employed in radio, telecommunications, computers and other electronicapplications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors.

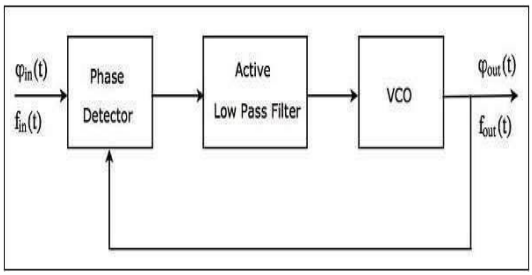

Fig1. Block Diagram of PLL

2.1 Phase Detector

The two inputs of the phase detector are the reference input and the feedback from the VCO. The PD output controls the VCO such that the phase difference between the two inputs is held constant, making it a negative feedback system. There are several types of phase detectors in the two main categories of analog and digital. Different types of phase detectors have different performance characteristic

For instance, the frequency mixer produces harmonics that adds complexity in applications where spectral purity of the VCO signal is important. In these applications the more complex digital phase detectors are used which do not have as severe a reference spur component on their output. Also, when in lock, the steady-state phase difference at the inputs using this type of phasedetector is near 90 degrees. The actual difference is determined by the DC loop gain.

2.2 Loop Filter

The block commonly called the PLL loop filter, usually a low pass filter generally has two distinct functions . The primary function is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at startup. Common considerations are the range over which the loopcan achieve lock (pull-in range, lock range or capture range), how fast the loop achieves lock (lock time, lock- up time or settling time) and damping behavior.

The design of this block can be dominated by either of these considerations, or can be a complex processjuggling the interactions of the two. Typical trade-offs are:increasing the bandwidth usually degrades the stability or too much damping for better stability will reduce the speed and increase settling time. Often also the phase- noise is affected.

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2.3 Voltage Control Oscillator

All phase-locked loops employ an oscillator element with variable frequency capability. This can be an analog VCO either driven by analog circuitry in the case of an APLL or driven digitally through the use of a digital-to-analog converter as is the case for some DPLL designs. Pure digital oscillators such as a numerically controlled oscillator are used in ADPLLs

OVERVIEW OF ADPLL:

Figure 2 shows the top level of the ADPLL circuit that is being shown. The top level is composed of a number of functional blocks, including a TDC circuit, a decoder for the TDC circuit, a phase detector, a basic digital glitch filter, a controller, a DCO, and a frequency divider. After two reference clock cycles, the TDC circuit gives the controller the length of half the reference signal'speriod when the ADPLL circuit is activated. After the controller outputs a coarse-tuning code, the DCO then produces the corresponding output frequency.

The DCO produces the corresponding output frequency once the controller produces a coarse-tuning code for it. The state machine in the Control block switches the circuit into the mode of tracking output frequency and phase acquisition after the TDC circuit has finished running. Depending on the phase difference between the reference signal CLK REF and the signal CLK DIV from the DCO output and divided by N in the Divider block, the phase detector outputs phase error signals UP or DN. The DCO fine- tuning code is modifiedby the controller when it receives UP or DN signals from the phase detector. They combine to create a closed loop.

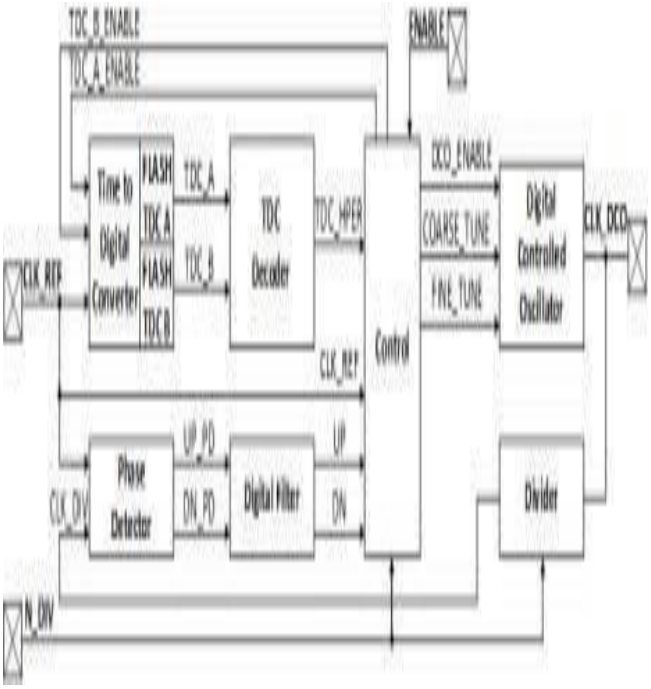

Figure 2. The Top level Of ADPLL Circuit

The Digital Controlled Oscillator serves as the ADPLLcircuit's motor (Fig. 2). It is the main power user in the ADPLL circuit and is in charge of producing the clock signal. Designing DCO on standard library cells was necessary to allow for the automatic production of the ADPLL circuit.

XILINX IMPLEMENTATION OF RTL SCHEMATIC:

In digital circuit design, register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals. Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived.

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Design at the RTL level is typical practice in modern digital design.
Unlike in software compiler design, where the register-transfer level is an intermediate representation and at the lowest level, the RTL level is the usual input that circuit designers operate on. Designing DCO on standard library cells was necessary to allow for the automatic production of the ADPLL circuit.

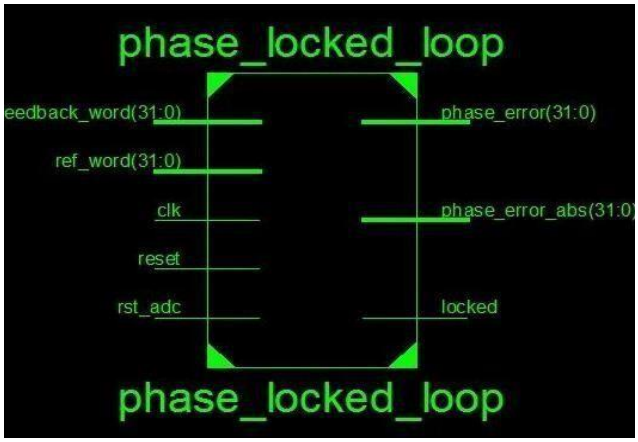

Figure 3. **SCREENSHOT OF RTL SCHEMATICUSING XILINX**

WORKING:
A 32 bit counter is also present in addition to the NANDgate in order to measure the phase error. The reference signal ref _word serves as the counter's reset (negative logic), while the NAND gate output ref_word serves as the counter's clear signal.
In reality, the signal ref _word comes from the digital controlled oscillator as a feedback signal. The ISim simulator's feedback _word and ref _word inputs have been forced in order to evaluate the functionality of this model. The counter runs along the clock's positive edge.

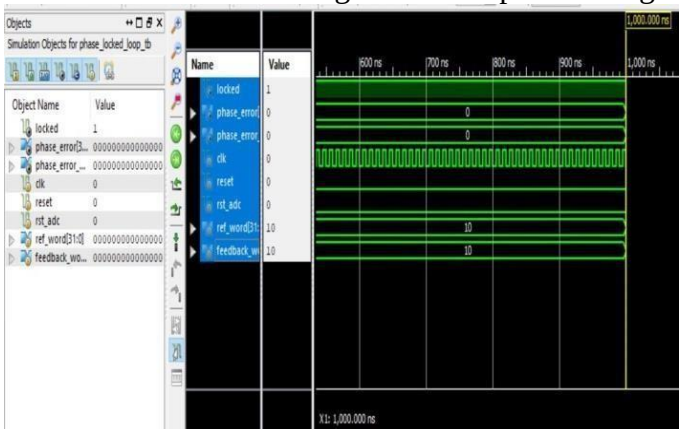

Figure 4. SCREENSHOT OF DIGITAL PHASELOCKED LOOP USING XILINX

3. SIMULATION AND RESULTS

The ADPLL circuit that is being presented was created using common library cells. Two-input NAND, inverter, tri-state buffer for fine-tuning DCO, and standardFlip-flop D trigger are the primary cells that makeup the critical building blocks of the DCO, TDC, and phase detector. The circuit in RTL is described using Verilog HDL. The outcomes of the RTL simulation of the ADPLLcircuit are displayed in Fig. 5. The reference signal's frequency is 20 MHz, and the frequency multiplier N is 16. As a result, 320 MHz is the output frequency.
These results demonstrate that the TDC produces the code word COARSE TUNE for two reference clock cycles. After the TDC operation is finished, the required output frequency is used to turn on the DCO circuit.

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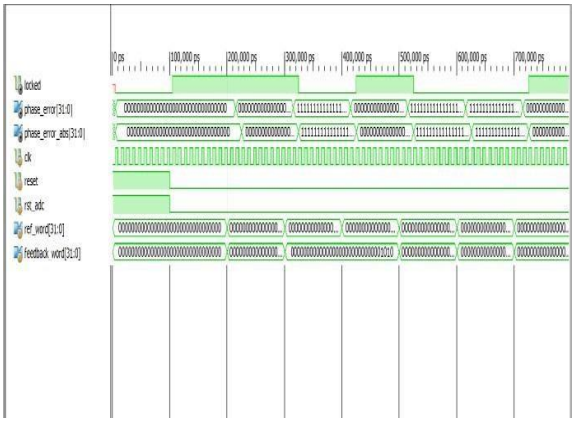

Figure 5. RESULTS OF THE RTLSIMULATION ADPLL CIRCUIT.

TABLE 1 : SIMULATION RESULTS

	DCO Coarse-tuning	**DCO Fine- tuning**	**Operatingrange**
Best case	130ps	21ps	286 – 722MHZ
Typicalcase	181ps	28ps	196 – 498 MHZ
Worstcase	306ps	62ps	113 – 286MHZ

CONCLUSION AND FUTURE WORK

In this paper, a fast-lock ADPLL circuit is presented. A two-level TDC circuit uses two reference clock cycles to perform the frequency search. The two flip-flops' phase detectors are in charge of acquiring the phase. With built-in ECO modes for speedy entrance into the working mode, this design is practical for low-power circuits. The project was a really nice learning experience. Although there are still many concepts and improvements to learn, this projectcovers the fundamentals of an all-digital PLL implementation. Using a complete bespoke design might enhance the design. Implementing a clock independent Digital Control Oscillator and swapping Loop Filter for a Time to Digital Converter will allow the extra clock input to be eliminated (TDC). The PLLcan be created for a specific application, such as GSM,WiMax, etc.

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