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Optimization of Synchronizers with Comparison

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Abstract

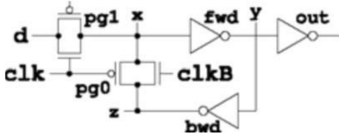
Real-world synchronizer circuit failure probabilities can be calculated using bisection with restarts[1]. Building on the bisection with restarts technique, further subsequent research [2] demonstrated how lime- varying, linear dynamics can be obtained for non-linear synchronizer circuits. Here, we demonstrate how the component- wise contributions to the synchronizer performance of this linear model can be separated. This makes it possible for the device's dimensions to be automatically optimized to reduce the likelihood of failure. In order to compare existing designs fairly, we can optimize each circuit before comparing them. The component- wise study demonstrates how each device contributes to metastability resolution over the allocated synchronization time, which clarifies the variations between designs.

Keywords: Synchronizer, bisection methods, time-varying linear dynamics, optimization, synchronization time.

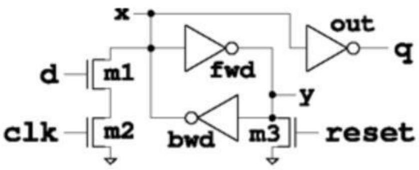
Introduction

Synchronizers are a common component of contemporary integrated circuits. Most semiconductors have a lot of clock domains that frequently operate at various frequencies to maximize power efficiency and performance. An interface between these domains needs synchronizers. Asynchronous communication networks are employed in Globally- Asynchronous, Locally-Synchronous (GALS) designs [3]-[5] to connect synchronous andasynchronous modules, and synchronizersare necessary for signals entering synchronous domains. At the interfaces between off-chip I/O links and on-chip modules, synchronizers are also utilized. Thousands or even hundreds ofsynchronizers can be found on large chips. Each synchronization procedures must havefailure probabilities between 10^{-15} and 10^{-25}or less in order to achieve acceptable reliability.

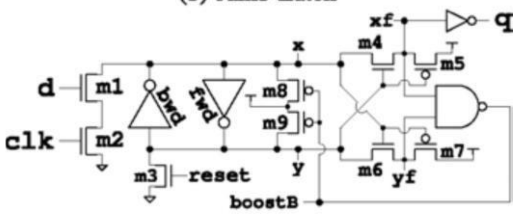
This paper adds two substantial expansions to [2]. Secondly, we note that the linearmodel from [2] can be further broken down into a linear combination of contributions from the various circuit components. Hence, we can explain how each transistor or logic gate contributes to the "instantaneous gain" of the synchronizer as a whole as well as the gain as a whole.



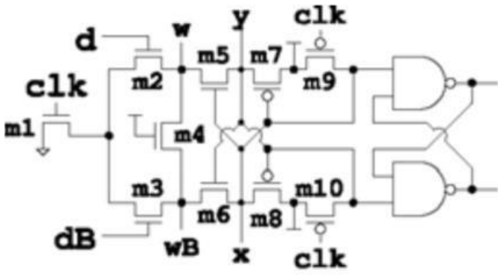
(a) Pass gate latch



(b) Jamb Latch



(c) Robust Synchronizer



(d) StrongArm Latch

Fig 1. Latches for synchronizers studied in this paper.

Section IV builds on this and shows how, given the contribution of each transistor to metastability resolution, we can automatically compute the derivative of thefailure probability with respect to transistor parameters, in particular, device width. This enables automatic optimization ofdevice size and comparison of different synchronizer circuits. Using this approach, Section, V presents a comparison of synchronizer constructed from pass-gate latches, one built from jamb latches, the robust-synchronizer circuit proposed in [8],and a synchronizer based on the Strong Armlatch [9].

II. RELATED WORK

II.1 Four latches**:**

The four sample synchronizer circuits used in this paper are shown in Figure 1 (note: inall schematics, signal B indicates the logicalnegation of signal). A pass-gate latch is depicted in Figure1a. Data values flow fromnode d through nodes x and y to the output q while clk is high; the latch is visible. In contrast, the fwd and bwd inverters form a loop when clk is low, and q maintains the value that d had at the falling edge of clk.

A jamb latch [10], as seen in Figure lb, makesan effort to enhance the synchronizer's performance by separating the pass-gate from the feedback loop of the two inverters. Instead, by asserting a high value on the reset input, each latch in the synchronizer isfirst put into a pre-determined, reset state. The latch is "one catching" if d and clk are both high because node x is pulled down bytransistors ml and m2 and node q goes high as a result. Because NMOS and PMOS devices can vary differently under PVT (process, voltage, and temperature) variation, care must be taken to ensure that the latch will function properly for all device parameters and operating conditions.

The "robust synchronizer" from [8] is depicted in Figure1c. A metastability filter is made up of the transistors m4 through m7. Keep in mind that m4 and m6 are in cut-off until node x's voltage is at least one NMOS threshold lower than node y's. The voltages at nodes x and y will be virtually equal when the cross-coupled inverters, fwd and bwd, are in metastability, and nodes xf (i.e., x "filtered") and it will be high. The resolved value is produced on q when the cross-coupled pair exits metastability. Either xf or yf drops low, while the other remains high. We now examine the latch's metastable behavior in more detail. As aresult, the NMOS transistors in these inverters have a higher gate-to-source voltage. The pace of metastability resolution is improved because transistor transconductance improves with gate- to-source voltage. The average impact on power consumption is minimal since the additional current is only used while the cross-coupled inverters are in a metastable state.

Last but not least, Figure 1d displays the Strong Arm latch from [9]. A timed sense amplifier is essentially what the latch is.Transistors m9 and ml 0 respectively precharge nodes x and y high when clk is low. Any difference between the complementary input signals, d and dB, on an upward rising edge results in a difference between the voltages on nodes w and wB. As a result, x and y eventually settle into opposing states. The state of the RS latch, which is made up of two NAND gates, is determined by the settling of x and y. This RS latch maintains its status even if clk drops again. Hence, a positive edge triggered flip-flop is implemented by theStrong Arm latch. It should be noted that the flip-flop is implemented using two latches in the other configurations in the figure 1.

II.2. Synchronizer Analysis

The earliest studies on the analysis ofmetastability in synchronizers were done by Kinnement & Edwards [11] and Molnar & Chaney [12]. Each individual latch was the subject of early synchronizer analysis. Examples include Kinniment and Woods[13] and Couranz and Wann [6]. This results in a theoretical analysis where:

$$P\{fail\}=T_w f_{clk} e^{-ts/r} \qquad (1)$$

The Tw(input window),fclk(clock frequency),ts(settlement time), and "r" refer to the metastability resolution time- constant of the bistable element in the latch, such as a pair of cross-coupled inverters, and P{failure} is the probability of a synchronizer failure for a single transition of its input. By locating the bistable element's metastable point, a linear, small- signal circuit model may be derived at this location, and its greatest eigenvalue can be used to calculate the parameter r. Tw is frequently defined as the range of input transition periods that obstructs the latch's set-up and hold window. In practice, it is an empirical correction term to account for everything else that happens during synchronization other than the bistable element loitering near its metastablepoint. Further elaboration of these single- latch models and their application to severalpractical synchronizer circuits is given. Real synchronizers are made up of manylatches. These circuits are time-varying dynamical systems, and the clock phase changes affect the circuit dynamics. Thefollowing technique (which assumes a low-to-high transition on d near the sampling clock edge) is the foundation of the bisection with restarts algorithm [1], which is used to discover metastability failures forsynchronizer circuits:

- Identify an input for which the circuit settles to output a low value by a specified sampling time, tcrit. Call this input tlo--notethat the synchronizer settles low for anyinput transition time > tlo.
- Identify another input, thi such that the synchronizer settles high at tcrit , when the input transitiontime is

< thi- Note that thi < tlo

- Perform a bisection search starting with thi and tlo, as the, endpoints of the search interval to find an input, tfail forwhich the circuit does not produce a valid logical output.-

This bisection model can help withunderstanding how synchronizers work, butit is difficult to implement with circuit simulators like HSPICE [7] because the numerical computations become unreliable for inputs close to "perfect" metastability, which can lead to conflicting findings. The key finding of the bisection with restartstechnique is that bisection can locate two very similar starting conditions, where one results in the synchronizer settling low and the other results in it settling high. As the simulation goes on, these two trajectories will separate from one another.

In order to use the states of the synchronizer for the two trajectories at time trestart as initial conditions for a new round of bisection, the method finds a restart time when the trajectories have drifted sufficiently. Each of these rounds is referred to as an epoch.

Time trestart is also selected to allow for theconstruction of a small-signal linear model along the trajectory. These small-signal models are implicit in [1], where the ratio ofthe voltage difference for the trajectories at the start and end of each epoch is used to estimate the "time-to-voltage" gain of the starting epoch. The synchronizer's overall time-to- voltage gain [15], [16] can be calculated by multiplying these ratios. Assuming that input transitions are uniformly randomly distributed over the clock period, this time-to- voltage gain can be used to determine the synchronizerfailure probability.

[2] This model serves as the foundation for the current work, so we will review their key findings here. A system of ordinary differential equations (also known as an ODE) can be used to simulate a circuit.

where *v(t)* is the voltage state at time *t; f* is the circuit model, derived using modified- nodal analysis; andv0 is the initial voltages state of the circuit. The derivative function,*f* is time varying to mode] external inputs such as *d,* the signal to be synchronized, and the clock. We write d(t,tin) to denote the data input signal; tin is a parameter that gives the time of the input transition. For the sake of simplicity, we define a signal transition as occurring when a signal passes the halfway point between ground and Vdd.Similarly, we set the synchronizer metastable by writing clk(t,P) to the valueof a clock with period P at time t; we presum that the clock edge of interest happens at time t = 0. To resolve metastability by the deadline, tcrit, the method of [2] computes a unit vector, u(t), that describes the "useful" component of the voltage vector at time t. This is the direction for the voltage vector v(t) at time t. A synchronizer's time-to- voltage gain is described asfollows:

$$g(t) = \frac{\partial}{\partial t_{\text{in}}} u(t)^T \mathbf{v}(t)$$

$$\begin{aligned} \tfrac{d}{dt} g(t) &= \lambda(t) g(t) + \rho(t) \\ lim_{t \to -\infty} g(t) &= 0 \end{aligned} \tag{4}$$

The instantaneous gain of the synchronizer is intuitively given by λ(t) because of positive feedback in the synchronizer circuit. The initial transformation of the input transition time, t_{in}, into the voltage state of the circuit at time t is modelled by the function ρ(t). While Equation 4 would be prettier if we could assume g(0) = 0, the synchronizer state may, in fact, depend on the behaviour of d slightly before the initial clock edge. In practice, we can assume g(t)=0 when t is a few gate delays before the initial clock edge.

$$\begin{aligned} \tfrac{d}{dt} \mathbf{v}(t) &= f(\mathbf{v}(t), t) \\ \mathbf{v}(0) &= \mathbf{v}_0 \end{aligned} \tag{5}$$

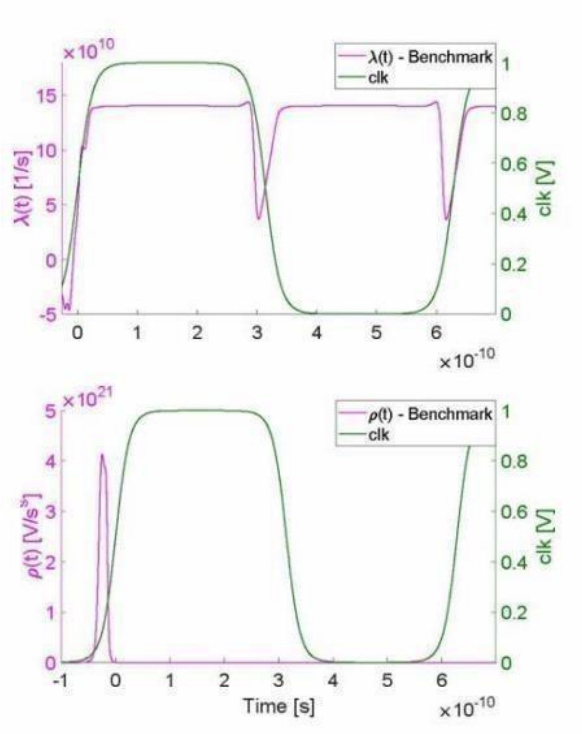


Fig 2: h(t) and p(t) for a 2 flip-flop, pass-gatesynchronizer

With a two-flip-flop synchronizer, shown in Figure 2, p(t) and λ(t) are shown. Each flip-flop is made up of two pass- gate latches that are transparent when the clk polarity is switched. The inhomogeneous portion, p(t),quickly approaches zero. The keycharacteristics of the synchronizer are captured by the homogeneous coefficient, λ(t). To illustrate the implications of metastability "travelling" from one latch to the next, consider how λ(t) dips at eachclock- edge. In the following section, we demonstrate how λ(t) can be broken down into the sum of contributions of the various synchronizers parts. This decompositionserves as the foundation for the optimization strategy presented in Part IV and is a potent tool for comprehending the reasons behind synchronizer behavior.

III. ELEMENT WISE METASTABILITY ANALYSIS

The main finding of our research is that the time derivative of the voltage state and the Jacobian operator for this derivative can be represented as simple sums of the contributions from the circuit components when employing modified-nodal analysis,the most popular approach of circuit analysis. We start with a few preliminaries on the formulation of the circuit model. Section III.1 sketches the key parts in the derivation of *g(r)* from [2] that we build upon in our element-wise analysis - a reader who wants more details is referred to[2].We then show how *g(t) can* be expressed in a element-wise form, and shown an example using the pass-gate latch.

III .1. Preliminaries

As written in Equation 2 A circuit's timeevolution can be expressed as d/dt v = f (v,t). Circuits with MOSFET transistors, capacitors, and either constant or time- varying voltage sources are taken into consideration in this work (e.g. for clk, d, and Vdd). To represent the current flowing from the transistors into each node of the circuit, we write I_{fet}(v,t). Because some circuit nodes are connected to voltagesources that are not included in the state- vector v and instead have values that are calculated from the value oft, the function Ifet(v,t) depends on 1. The capacitance matrix for the circuit is represented by the letters C(v,t). C(v,t) i,j is the capacitance between nodes I and j at time t for the i≠j system, and C(v,t)i,i is the total capacitance connected to node i. MOSFETs' inter- terminal capacitances are non- linear functions of the terminal voltages. In order to account for nodes that are connected to voltage sources, C is a function of v and depends on t. According to Kirchoff'scurrent law, the current flowing from the node into the capacitors is C(v,t) d/dt v(t), which must equal I_{fet}(v,t),Thus,

$$\frac{d}{dt}\mathbf{v(t)= \ C\,(v,t\,)^{-1}\ I_{fet}(v,t)} \quad \mathbf{(5)}$$

Let *f(v,t)* = *C(v,t)*$^{-1}$ Ifet(v,t) asdescribed above.

The Jacobian operator for f plays a central rolein the analysis:

$$\mathbf{Jac(f,v,t)_{i,j} \ = d/dvjf(v,t)_{I}} \qquad \mathbf{(6)}$$

We write *Jf(t)* as a short hand for *Jac(f,v(t),t)*.

We now summarize key quantities forcomputing λ*(t)* and g(t)

- S(t1,t2): how a change in the circuitstate at time t1affects the circuit's state at time t2 S(t1,t2) is a n×n matrix
- Tcrit: the time at which the synchronizer output must be well-defined and settled. Teola: time of the "end-of- linear-analysis". We choose teola to satisfy:

1. At time teola, the settle-low and settle-high trajectories are sufficientlyseparated so that numerical integration of the circuit model correctly resolves theiroutcomes for times t ≥ teola, and
2. These trajectories are close enough so that small- signal linear analysis is valid for t ≤teola.

- u(t): a unit vector corresponding to "useful" separation of trajectories at time teola. Typically, we use thedifferencebetween the inverter outputs of the final (or next-to-last) cross- coupled inverter pair.
- u(t): The pre-image of u at time t for t≤ teola - a unit vector. Intuitively, u(t) is the vector that describes what part of β(t) is "useful" for synchronizer resolution attime teola (and thus at tcrit).

$$u(t) \;=\; \left(S(t,t_{\text{eola}})^{-1}\tilde{u}\right)\left\|S(t,t_{\text{eola}})^{-1}\tilde{u}\right\|^{-1}$$

λ (t) and p(t): We now have the ingredients for the simple model for g(t):

While p(t) is essential near the initial clock edge to establish the initial imbalance of the synchronizer, for practical synchronizers, p(t) rapidly approaches 0 after that clock edge - see Figure 2, Thus, most of our attention will be on decomposing λ(t).

III.2. Computing Failure Probabilities

While [2] offered a thorough framework for analysing synchronizer behaviour, it lacked a straightforward method for calculating the likelihood of synchronizer failure. Equation 1 in this section is derivedfrom Equation 7.

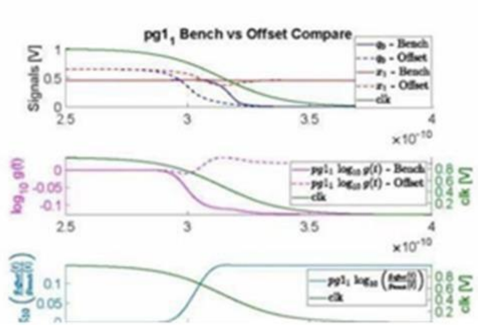
(8)

$$P\{\text{failure}\} = \frac{2\Delta V_{\text{eola}} f_{clk}}{g(t_{\text{eola}})}$$

Consider the simple case of a single latch synchronizer. Figure 3 shows *g(t)* for a single pass-gate latch. We observe that the slope of log g(t) is nearly constant for the settling time and use a least-squaresregression to obtain go and λo such that:

$$\begin{aligned} J_{f,d}(t) &= \\ &-C(\mathbf{v}(t),t)^{-1}\text{Jac}(C_d,\mathbf{v}(t),t)C(\mathbf{v}(t),t)^{-1}I_{fet}(\mathbf{v}(t),t) \\ &+C(\mathbf{v}(t),t)^{-1}\text{Jac}(I_{fet,d},\mathbf{v}(t),t) \\ J_{f,D}(t) &= \Sigma_{d\in D} J_{f,d}(t) \\ \lambda_d(t) &= u^T(t)J_{f,d}(t)u(t) \\ \lambda_D(t) &= u^T(t)J_{f,D}(t)u(t) \end{aligned}$$

$$g(t) \approx g_0 e^{\lambda_0 t}$$



Let $v^{lo}(t)$ (resp. $v^{hi}(t)$) denote the trajectories that settle low (resp. high) just in time, and In the linear region for log g(t), we get

$$\Delta \mathbf{v}(t) \approx 2\Delta V_{\text{eola}} e^{\lambda_0 (t - t_{\text{eola}})}$$

$$\begin{aligned} \tau &= 1/\lambda_0 \\ \Delta V_{\text{crit}} &= 2\Delta V_{\text{eola}} e^{\lambda_0 (t - t_{\text{eola}})} \\ T_w &= \Delta V_{\text{crit}}/g_0 \end{aligned} \qquad (10)$$

Equation 1 is produced by substitutingEquations 9 and 11 into Equation 8. In a graph, the value of g(t) produced by extending the line-of-best-fit back to t= 0 is known as g_o.

Fig.3: Pass-gate latch gain and line-of-best-fit

III.3. Element-wise lambda(t) and g(t)

From Equation 5,

but we need to be careful about the notation: C(v,t) isa n x n vector; therefore

$$\begin{aligned} J_f(t) &= \\ &-C(\mathbf{v}(t),t)^{-1}\text{Jac}(C,\mathbf{v}(t),t)C(\mathbf{v}(t),t)^{-1}I_{fet}(\mathbf{v}(t),t) \\ &+C(\mathbf{v}(t),t)^{-1}\text{Jac}(I_{fet},\mathbf{v}(t),t) \end{aligned}$$

Jac(C,v,t) is a n x n x n tensor. To make thecalculation explicit, let we define Cd and CD in the same way, and define:

This figure shows pgl. of stage I which connects stage 0 and stage 1 of a pass-gate flip-flop.

$$\begin{aligned} \lambda(t) &= u(t)^T J_f(t) u(t) \\ \rho(t) &= u(t)^T \frac{\partial}{\partial t_{in}} f(\mathbf{v},t) \\ g(t) &= u(t)^T \beta(t) \\ \frac{d}{dt} g(t) &= \lambda(t) g(t) + \rho(t) \end{aligned}$$

Fig.4.:Pass-gate synchronizer with offset coupling inverters

The signal go is the output of inverter out from Figure la, pgl1 and x1 is the pass-gate and node x of the following pass-gate latch in the chain.

Observing that p(t) converges to 0 after the initial clock edge, we chose thomo So that |ρ(t)|«|λ(t)g(t)| for t≥thomo. From equation 7, we get

Device d's contribution to the resolution of metastability at time t is described by the functions λd(t).λd(t) calculates the effect of agate or other circuit module by selecting D as its constituent devices. The cumulative contribution of a device or module is described by the functions gd(t) and

$$g(t) \approx g(t_{\text{homo}})e^{\int_{z=t_{\text{homo}}}^{t}\lambda(z)dz} \qquad (15)$$

$$\begin{aligned} g_d(t) &\approx e^{\int_{z=t_{\text{homo}}}^{t}\lambda_d(z)dz} \\ g_D(t) &\approx \prod_{d\in D} g_d(t) \end{aligned}$$

gD(t). Here is a straightforward example to demonstrate this. Part IV expands on the per-device analysis for automatic device sizing.

III.4. Active Pass-Gates

Now it’s time for a short narrative. You can skip to Section IV if you don't enjoy stories. According to some synchronizer lore, if a synchronizer had latches with differing metastable voltages, the first latch would have to exit metastability before the second latch became opaque for metastability to shift from one latch to the next. According to folklore, the latch state is"exiting" rather than "trapped at metastability," which should lower the likelihood of failure.

$$J_C(\mathbf{v},t,j) \;=\; \tfrac{\partial}{\partial \mathbf{v}_j}C(\mathbf{v},t)$$

then

$$-C(\mathbf{v}(t),t)^{-1}\mathrm{Jac}(C,\mathbf{v}(t),t)C(\mathbf{v}(t),t)^{-1}I_{fet}(\mathbf{v}(t),t)$$

is the $n\times n$ matrix whose j^{th} column is

$$J_c(\mathbf{v}(t),t,j)C(\mathbf{v}(t),t)^{-1}I_{fet}(\mathbf{v}(t),t)$$

Of course, we knew this was wrong. The gain-bandwidth product of the cross- coupled inverters is highest at or near their balance point. When the first latch exits metastability early to establish metastability in the next latch, gain will be lost. We set- up a test case by using coupling inverters (out in Figure 1a) with a different P:N sizing ratio than the cross- couple pair. Imagine our horror when this resulted in a slight reduction in the failure probability.

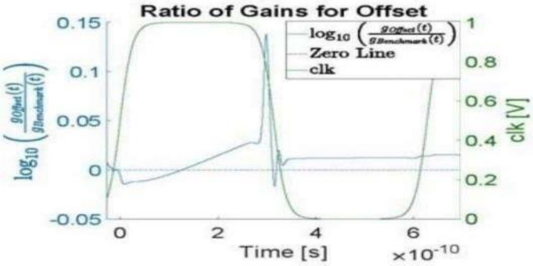


Fig. 5.: g(t) for a pass-gate synchronizer,with and without offset

The plot of A(t) and the voltage waveforms confirmed that the latch before the offset inverter does indeed exit metastability early(see the plots for q in the top panel ofFigure 4).

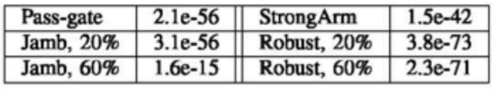
See the charts for q in the top panel ofFigure 4 for evidence that the latch before the offset inverter does indeed leave metastability early. As seen in the middle panel of Figure 4, the pgl pass-gates favored the design with an offset in the inverter thresholds (the sizing with matchedP:N ratios is called "bench" in the figure).Because Vgs is so near to the threshold voltage and the body effect just makes things worse, it turns out that thepass-gates conduct fairly weakly when theirsources are at the metastable voltage for thesynchronizer. The source voltages can be swung closer to ground to improve the efficiency of the NMOS transistors. We were even more shocked to see a tiny window of time where the pass-gate contributed positively to the instantaneous gain—it was functioning as an amplifier! Yes, it was. The source of the NMOS device was moving towards ground, andthe gate was almost at Vdd. The NMOS transistor operates as a common gate amplifier when the voltage on q is much below clk.

There are anomalies to find even after the surprise amplifier. Figure 5 displays the twodesigns g(t) values. The coupling inverter exhibits a lower Miller capacitance in theoffset case because it has a smaller gain, which causes the gain to initially increase more quickly for the offset design. The pass-gate pgl in the second latch, as previously mentioned, is what causes the upward surge.We have not pinpointed the precise reason of the downward spike that occurs in thecross-coupled pair of the second latch. Allof them together gave the synchronizer with the offset a tiny advantage. This experiment served as a reminder of how frequently transistors in synchronizers operate veryclose to their cut-off positions. Unless these are identified, the performance of the synchronizer may be significantly different than expected.

VI. AUTOMATIC TRANSISTORSIZING

The gradient-descent method for optimising transistor widths to reduce failureprobability is presented in this section. The fundamental strategy is straightforward: foreach transistor, ascertain how altering itswidth affects its failure probability; modify transistor widths to lower the failure probability; and repeat until theimprovements are below a user- specified threshold. To be more precise, we (I) create the ODE model for the circuit with w as a parameter, which is a vector of transistor widths; (II) calculate the gradient of P{fail}with respect to w; and (III) apply gradient steps up until the improvement threshold is attained. Three issues arise with this approach: (1) *P{fail}* tends to have an exponential dependence on parameters which undermines the linear- approximations that underlie gradient descent optimization; (2) Jacobian matrices are used throughout analysis, taking the derivatives of these withrespect to a vector results in a large numberof tensor operations; and (3) optimization needs correctness constraints to avoid producing designs that are dangerously close to being wrong.

To avoid the exponential sensitivities of P{fail}, we formulate the problem as one ofmaximizing logg(teola)-RewritingEquation 15, we get



Pass-gate	2.1e-56	StrongArm	1.5e-42
Jamb, 20%	3.1e-56	Robust, 20%	3.8e-73
Jamb, 60%	1.6e-15	Robust, 60%	2.3e-71

$$\log g(t) \quad \approx \quad \log g(t_{\mathrm{homo}}) + \sum_{d \in \mathcal{D}} \int_{z=t_{\mathrm{homo}}}^{t} \lambda_d(z)dz$$

More challenging are the tensors that appearwhen computing the derivatives of Jacobian matrices with respect to the width vector. MATLAB's automatic - differentiation (AD) package fromINTLAB [17] is used in our implementation. We had to write our own code for tensor operations, despite the fact that this INTLAB offers good supportfor operations with vectors and matrices. Since our code is based on the INTLAB core, it is not affected by specifics of the device models used or the circuit being studied. The fact that INTLAB uses operator overloading to implement the forward AD algorithm is a more seriousflaw. This adds a slowing element to the code that, in our opinion, a backward algorithm could eliminate. Even though some work has been done onbackward AD for ODEs [18],[191]:[18] does not give some of the operationswe need, including Hessians; and [19] examines AD for higher-order derivatives but does not provide implementations.

As a final design constraint, we added requirements for the jamb-latch and robust synchronizer's correctness as well as a minimum transistor width and maximum overall width. A pull-down path (such asml and nit in Figures lb and 1c) must prevail in both configurations over the pull-ups in the inverter bwd. The fwd inverter and transistor m3 operate similarly. At eachoptimization step, the optimizer computes the minimum safe widths for thesetransistors, adds a user-specified margin, and adjusts the widths if needed to ensurea correct design.

V.SYNCHRONIZER COMPARISON

We applied the analysis methods outlined in the preceding sections. Our transistor models are a streamlined version of the EKV [21] with parameters that have been fitted to the PTM [22] 45nm model. Miller capacitances and other nonlinearcapacitances between signal nodes are included in our circuit models since the capacitance model accounts for nonlinearcapacitances between all terminal pairs of aMOSFET device. Our reported figures are for synchronizers that are running nearlytwice as quickly as they should be since ourmodels do not account for connectioncapacitance. This holds true for all of the designs, thus the relative performance comparisons shouldn't be much impacted. Two-flip flops make up everysynchronizer. Each latch in the Strong-Armlatch synchronizer implements a positive edge-triggered flip-flop, but in the other designs, each flip- flop is made up of two latches, with the master being updated when the clock is low and the slave being updated when the clock is high. To create designs that could work for a genuine cell- library, all latches for each synchronizer were optimised to have the same transistor dimensions. On the other hand, because we sought to evaluate the circuit design andnot the specifics of a particular set of design rules, we offered the optimizationmethod continuous possibilities of transistor widths. We established a total width budget of four times the number of transistors times the minimum width and a minimum width of 200nm for each transistor. With tcr it set to 120ps after the second rising clock edge, all designs were tested at 1.6GHz clock frequency.

The results are summarised in Table I. The NMOS pull-down networks must be able tooverwhelm a PMOS pull-up in order to enable the jamb latch and robust synchronizers. We optimised designs with a20% margin, which means the NMOS network can sink 20% more current than the minimum required, and a 60% margin to accommodate for PVT fluctuation. The strong synchronizer [8] comes out on top. According to the failure probability in Table I, the robust synchronizer's r should be around 4 ps, which logically equates to the 20.7 ps figure given in [8] for a 180nm implementation. Remarkably, the robustsynchronizer's foundation, the jamb-latch [10], performs quite poorly in the 45nmtechnology employed in this paper.

Below, we go over each design in greater depth. We used the pass-gate latch as our starting point because it isa straightforward design that is well-known to mostdesigners. All transistors in the inter stage coupling inverters and p g were reduced to their smallest size by the optimizer. Onpage 3, the transistors are a little bit bigger. We were astonished to find that pg1somewhat increases the gain of the synchronizer as metastability switches between latches, as discussed in Section 111.4.

The jamb latch delivered both an anticipatedoutcome and a surprise. The projected outcome was that when developed in a 45nm (or smaller) technology, the NMOS pull-down transistors would need to be quite large. The NMOS devices don't have a significant advantage over their PMOSequivalents because to velocity saturation. The main reason why the jamb latch design performs poorly is the wide widths of the NMOS transistors. We were surprised tofind out that there are two different ways to move metastability between latches based on the P:N ratio of the output inverter for each latch. When stage I is metastable, the "typical" condition is that the output inverterdrives the following d input of stage i+1 to avalue that is too low to switch the nextstage. When stage I resolves to raise d just as the timer for stage I+1 expires, metastability spreads. In the alternative scenario, when stage I is metastable, theoutput inverter of stage I is high enough to flip stage i+1. When stage I resolves to drive d low shortly after the clock for stage I+1 goes high, metastability spreads. As a result, stage I+1 experiences a runt pull-down pulse, which leads to metastability.

The jamb latch design and the resilient synchronizer both have two forms of metastability propagation. The fact that the optimizer uses minimal width pull-ups in the fwd and bwd inverters is a more intriguing finding. In the absence of metastability, those pull-ups guarantee accurate logical operation. Largertransistors ma and m9 offer substantiallyhigher pull-up current when resolving metastability since their gates are grounded by boost B. The inverters' tiny pull-ups make it possible for the pull- down networks, or ml, m2, and m3, to berelatively compact. Although it isn't mentioned in the publication, based on the transistor sizes utilized in C8], it appears that they were aware of this

characteristic. The discovery of an undocumented design feature made us very happy.
It was initially unexpected that the Strong Arrn design performed poorly because the Strong Arm is renowned for performing well and using little power in logiccircuits. It appears to be well suited for resolving metastability given its sense- amp approach. A closer look reveals that it has additional loads on both sides of the cross-coupled pair as well as additional series transistors on its pull -down paths, both of which cause problems.

V.CONCLUSIONS

We have presented the metastability analysismethods that quantify the contribution of each transistor and logic element of a synchronizer to the overall performance. In particular, the time-varying models from [2]can be decomposed into a sum of contributions from each component. We have implemented the algorithm and applied it to real synchronizer designs. Our techniques take into account the implications of non-linear circuit behaviourwhen metastability progresses across latches as well as the small-signal linearbehaviour of latches in metastability.
We demonstrated examples of how the pass-gates in a straightforward synchronizer can function as active amplifiers that aid in the metastability solution. We demonstrated that, depending on the transistor sizes in thelatch circuit, the well-known jamb latch canconvey metastability between stages in two qualitatively different ways.
Automatic device scaling is made possible by the capacity to take into account the contribution of each transistor to the resolution of the metastability. Thisallowed us to compare the designs and optimize four well- known synchronizer circuit topologies. We discovered design characteristics as a result that, to the best of our knowledge, have never been published. For instance, we found that Zhou's robust synchronizer's passive PMOS pull- ups [8] result in transistor size that significantly increases the design's resistance to PVT fluctuation, particularly 11/v IOS-vs-PMOSskew. The tolerance to low operating voltages is emphasized in Zhou's paper, although the advantage of tolerating PVT volatility is not mentioned.
Further research is needed in a number of areas. Initially, we want to build numerically integrable backwards automatic differentiation algorithms. The forward technique is now the bottleneck for optimization, and a backwards computationshould be able to reduce the time it takes to determine ideal transistor sizing by an order of magnitude. Currently, a full optimization run can take up to a day. We emphasize that our method successfully applies gradient descent to a numericallyintegrated result, where the objective function and gradient were computed using Aland the integrand was obtained using AD.A quicker optimizer would allow for more experiments, even though our current implementation shows that this deepintegration of scientific and symbolic computation is feasible. The wagging synchronizer [23], the pseudo-NMOS synchronizer [24], and the voltage- boosted synchronizer [25] are all in trigging possibilities.

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