International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Special Issue: 1 Volume No.7 April – 2023
DOI:10.46647/ijetms.2023.v07si01.102 ISSN: 2581-4621

Different SRAM Cell Topologies Analysis And Design Implementation

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Abstract- Now a day's semiconductor memories SRAMs are widely used in computer systems, microprocessors, microcontrollers and system on chips (SoCs) based equipment's. In this Project, We Design and analyze a diverse kind of SRAM cell Topologies. This Project revealing about the presentation of five SRAM cell geographies, which incorporate the customary 6T, 7T, 8T, 9T, and the 10T SRAM cell executions. Specifically, the spillage flows, spillage force, and read conduct of each SRAM cells are analyzed. In 10T SRAM cell usage results, diminished spillage force, and spillage current by 36% and 64% separately, the real strength is expanded by 13% over regular 6T, 7T, 8T, and 9T SRAM cells. Subsequently, the 10T SRAM consistently expends the least spillage force and spillage current; improve read solidness when contrasted with the 6T,7T, 8T and 9T SRAM cells. The point of this Project is to diminish the spillage power, spillage current and improve the read conduct of the distinctive SRAM cell structures utilizing rhythm device at 45nm innovation while keeping the peruse and compose get to a time and the force as low as could reasonably be expected.
Keywords: SRAM, Topology, Leakage Control Transistors, decoder.

I.INTRODUCTION

SRAM has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. SRAM and DRAM holds the data but both the operating conditions are different. DRAM needs that data to be refreshing or retain the data after a particular time but SRAMdoes not have this issue. SRAM does not required to be refresh periodically. SRAM is interconvertible in nature that means it does not hold the information in terms of data whenthe power is cut off completely. To refresh the DRAM periodically it requires additional circuits which make the DRAM slower and bulky. One more complication with the DRAM is its power consumption is also high as compare to SRAM. So the DRAM is less desirable as compare to SRAM. Due to these above reasons SRAM is widely used inSoCs due to ease of usability and high speed. The memory sizes of the Cache are improved with improvements which play a significant part in the use of microchips and thesystem-on-chip SRAMs are widely used for mobile applications as both on chip and offchip memories, because of their ease of use and low standby leakage. The main objective of this paper is evaluating performance in terms of Power consumption reduce quadratically and exponentially respectively with supply voltage. With the proliferation in the demand of low power devices like wireless sensor networks, implantable biomedical devices and other battery operated portable devices, power dissipation has become a key design constraint. Static Random Access Memory (SRAM) is the major contributor to the power dissipation, as they occupy significant portion of Systems-onChip (SoCs), and their portion will grow further in the future. The power consumption will increase as leakage rises exponentially therefore, necessary to minimize the power associated with SRAM in order to have a power efficient design. Reducing the supply voltage is a straight forward way to achieve power efficiency because the active and leakage power

II.LITERATURE SURVEY

The SRAM occupies the major area of a die in system-onchip (SoC) products and consumes significant amount of power. Hence, active and leakage-power-efficient SRAM designs need to be

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explored for longer operation of battery operated systems. There are two primary areas having strong potential of active and leakage power reduction (a) lowering the operating voltage which has quadratic dependency with active power (Pactive = α ∗C ∗V2 DD ∗ f) and linear relationship with leakage power, and (b) reduction in charging or discharging the capacitance of word and bit lines. It has been reported that up to 70% of the total active power is dissipated in charging or discharging of bitlines during read and write operations. The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. Solutions involving additional transistors, i.e., 8T, and 9T, 10T, Differential 10T have been explored to lower power consumption while reducing these adverse effects in the cell performance. We will therefore look into a couple of these SRAM Cells topologies that allow the analysis and simulations of different parameters at 90nm, 32nm and 45nm technology successfully on the basis of the power dissipation, speed and their temperature dependence with the area efficiency of the circuit.

6T SRAM CELL:

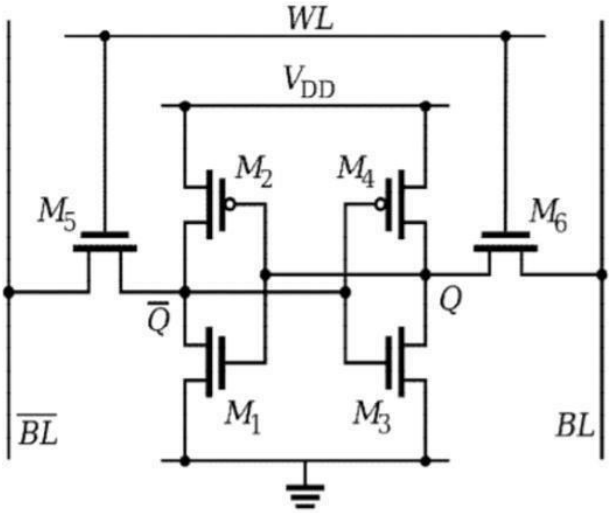
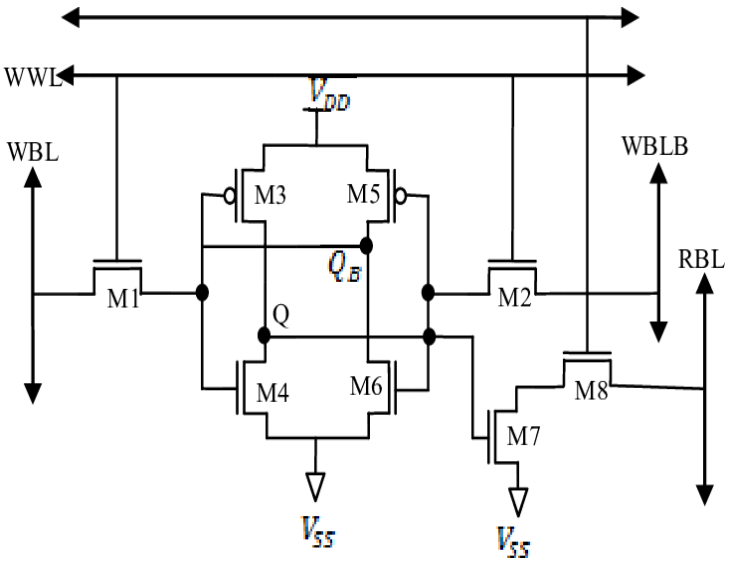


Fig: Schematic Diagram of 6T SRAM cell



The conventional SRAM cell made of 6 MOSFETs is the most basic SRAM cell. This cell consists of two access transistors and two cross-coupled inverters with a common read and write port. Asserting a high value to WL enables the access transistors for both read and writeoperations. For hold operation, WL is set to a low value.

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7T SRAM CELL:

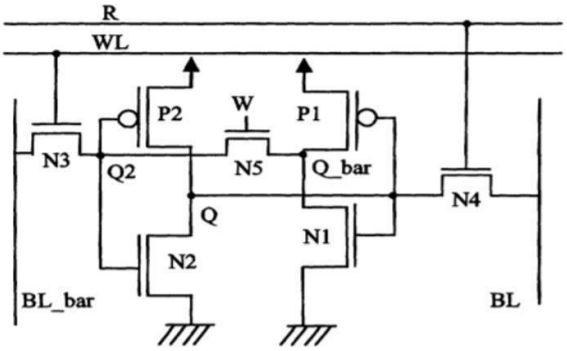

Fig: Schematic diagram of 7T SRAM cell

7T SRAM cell that has an additional NMOS transistorN5 as compared to the conventional 6T SRAM cell. The write operation in this cell depends on removing the feedback connection between the two inverter pairs before the write operation, and the transistor N5 serves the purpose of feedback connection and disconnection. For writing in this cell, N5 is turned OFF. During the read operation,the cell behaves like a conventional 6T SRAM cell with N5 in ON state.

8T SRAM CELL:

The 8T SRAM cell us**es** two NMOS access transistors extra, one read word line, and one read bit line compared to the conventional 6T SRAM cell to form the isolated read path. During the read operation

Fig: Schematic Diagram of 8T SRAM cell

data storing nodes are fully decoupled from the read bit line to enhance RSNM. 8T-SRAM cell uses a single-ended read scheme which reduces the swing of bitlines**.**

9T SRAM CELL :

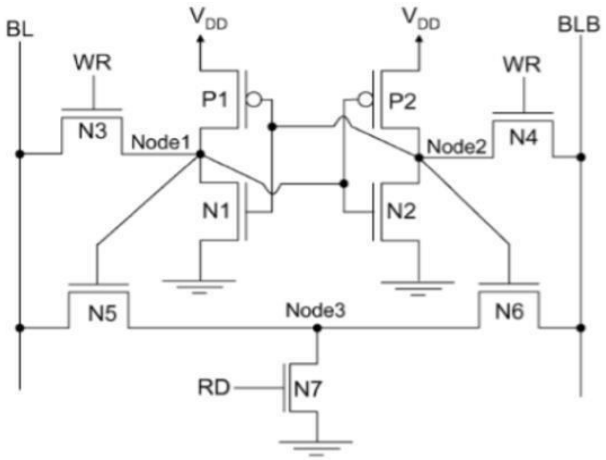

Fig: Schematic Diagram of 9T SRAM cell.

This cell is designed with the aim of improving stability and reducing power consumption. It can be viewed as a combination of two sub-circuits – the upper and lower sub-circuits. Theupper sub-circuit is responsible for data storage, and the lower sub-circuit contains transistors for bit line access and read access. This cell uses a separate read signal that controls the read access transistor N7.

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III.PROPOSED METHOD:-

10T SRAM CELL

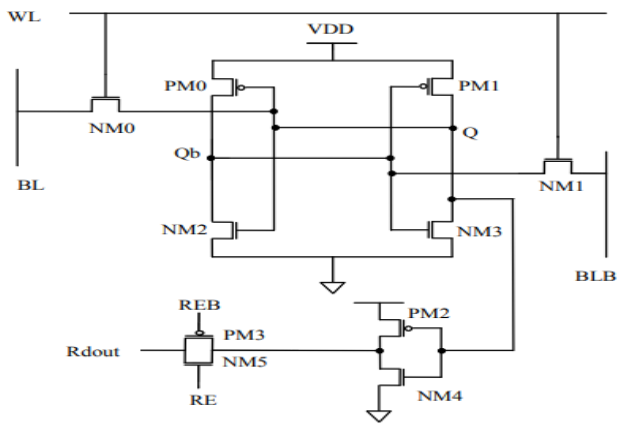

Fig: Schematic of 10T SRAM cell

A 10T SRAM cell is a type of memory cell used in static random-access memory (SRAM) circuits .It consists of ten transistors arranged in a cross-coupled configuration that enables the cell to store a single bit of data. The 10T SRAM cell has a higher stability than the more commonly used 6T SRAM cell, which only has six transistors.The 10T SRAM cell has two access transistors, two read assist transistors, two write assist transistors, and four pass transistors. The access transistors enable the cell to be accessed for reading or writing data

The 10-T (Transistor) static random access memory (SRAM) cell with reduced power and with improved static noise margin (SNM) is proposed. The 10-T SRAM employs a single bitline with dynamic feedback control which enhances the SNM at ultra low power.

However, radiation hardening techniques for memories are one of the bottle necks in providing fault tolerance .For many years, radiation-hardening designs techniques have been used to tolerate soft error in memories using standard commercial cmos foundary process,with no modification to the existing process or violation of design rules. Traditionally,these techniques can be divided into the following three subitem techniques. They are

- layout techniques employs main layout changes
- The first circuit level technique is trple modular redundancy which is used for mitigating seu
- The most common circuit level hardening are to add extra redundant transistors

Simulation tool:

Simulation for the Proposed Braun Multiplier using the Tanner EDA tool technology. All the PPA is implemented using the CMOS technique. The parameters considered for comparison are number of transistors and time delay. The integrated circuit is developed by the Tanner EDA tool. The various parameters are considered by this tool. In this software, the process was done by the four tools 1. Tanner Sedit: Schematic 2. Tanner T-spice: the SPICE simulation mechanism which is integrated with Tanner L-edit - a physical design tool to make the layout 4. Tanner W-edit–the waveform tool Simulation for the Proposed Braun Multiplier using the Tanner EDA tool technology. All the PPA is implemented using the CMOS technique. The parameters considered for comparison are number of transistors and time delay. The integrated circuit is developed by the Tanner EDA tool. The various parameters are considered by this tool. In this software, the process was done by the four tools 1. Tanner S-edit: Schematic 2. Tanner T-spice: the SPICE simulation mechanism which is integrated with Sedit, 3. Tanner L-edit - a physical design tool to make the layout, 4. Tanner W-edit–the waveform tool.

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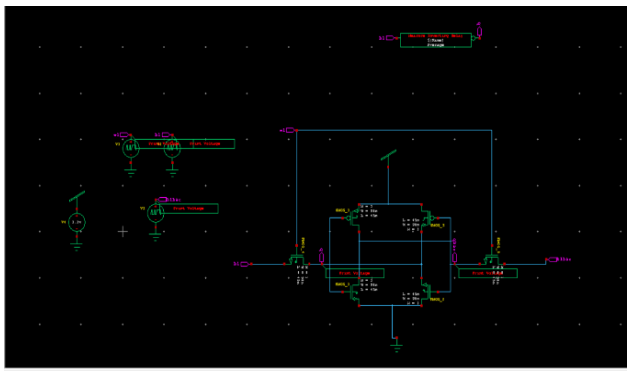
IV.EXPERIMENTAL RESULTS:

6T SRAM CELL



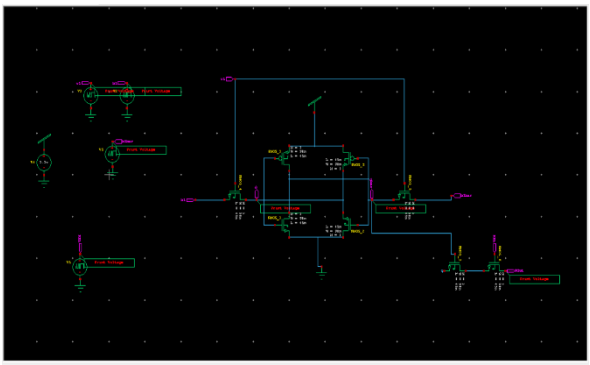
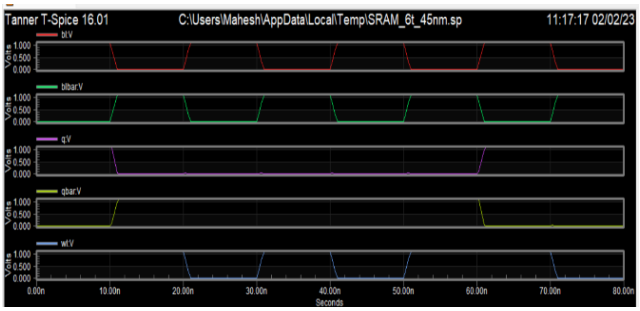


Fig: Schematic of 6T SRAM



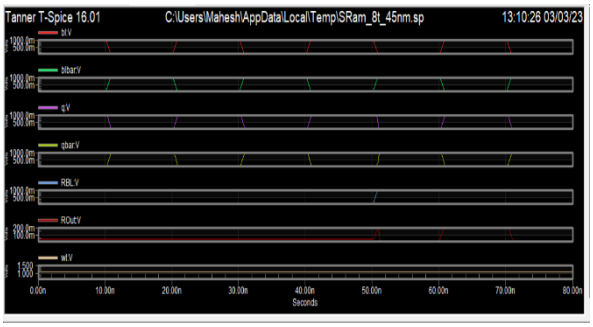
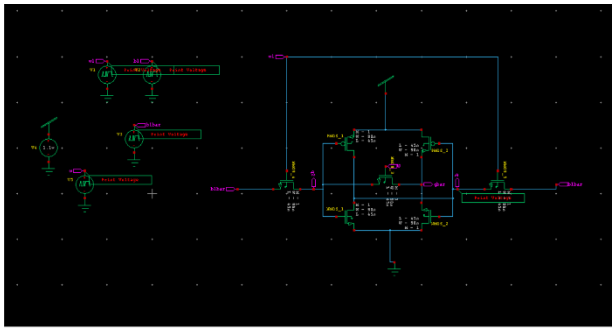


Fig:-waveform of 6T SRAM

7T SRAM CELL



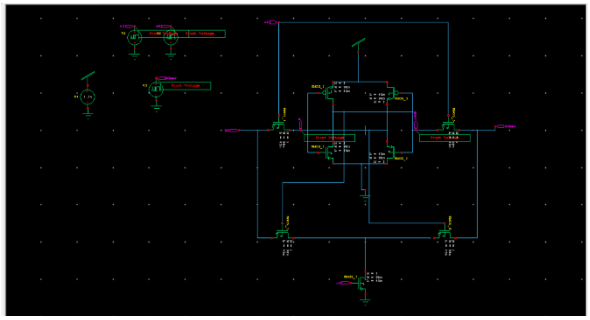


Fig:-Schematic of 7T SRAM cell

Fig:-waveform of 7t SRAM cell

8T SRAM CELL

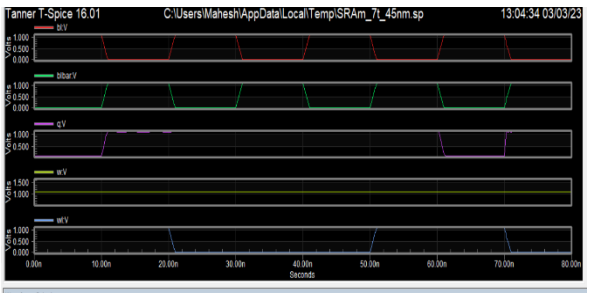


Fig: Schematic of 8T SRAM Cell

Fig:-waveform of 8T SRAM cell

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9T SRAM CELL

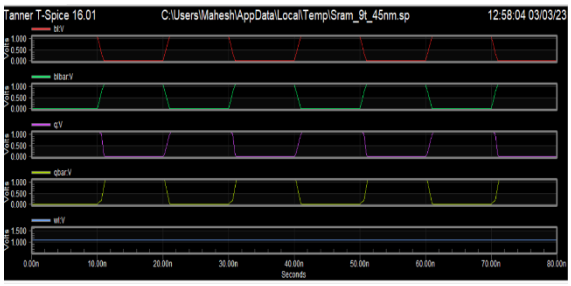
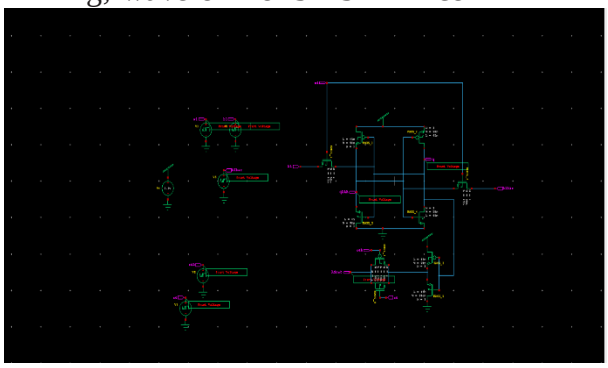


Fig:-Schematic of 9T SRAM Cell

Fig;-waveform of 9T SRAM cell



10T SRAM CELL:

Fig:-Schematic Of 10t SRAM Cell

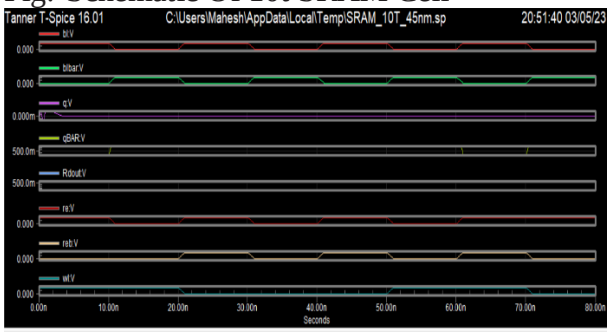


Fig: Waveform of 10T SRAM

Comparison of SRAM cells

s.no	parameter	6T	7T	8T	9T	10T
1	Technology	45 nm	45 nm	45 nm	45 nm	45 nm
2	Supply power	700 mv	700 mv	700 mv	700 mv	700 mv
3	power	19.1 nw	16.8 nw	24.4 nw	18.1 nw	12.1 nw

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4	**Read delay**	**110 ps**	**92.8ps**	**81.7 ps**	**84.4ps**	**50 ps**

V.Conclusion

In this project we design different type of SRAM cells. This project compares the performance of five different SRAM cell topologies, which include the conventional 6T, 7T, 8T, 9T and 10T SRAM cell implementations. In particular, the leakage currents, leakage power and read behavior of each SRAM cells are examined. The 10T SRAM is our proposed SRAM cell, in which a dedicated inverter and transmission gate are appended as a single-end read port. Even though 10T SRAM cell implementation results in a reported reduction in leakage power and leakage current by 36% and 64% respectively, the read stability is increased by 13% over conventional 6T, 7T, 8T and 9T SRAM cells. As a result, the 10T SRAM always consumes lowest leakage power and leakage current, improve read stability as compared to the 6T, 7T, 8T and 9T SRAM cells.

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DOI:10.46647/ijetms.2023.v07si01.102 ISSN: 2581-4621

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