

Comparative Analysis of Network Parameters using Noxim Simulator

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ABSTRACT

In the field of Network-on-Chip, simulation is one of the primary techniques used to examine and evaluate novel ideas. It is necessary to have simulation tools available that are frequently restricted to modelling particular network configurations in order to evaluate the performance and power figures of NoC and WiNoC systems. This article introduces Noxim, a SystemC-developed open, extendible, customizable, cycle-accurate NoC simulator that enables the analysis of the performance and power statistics of both established wired NoC and new WiNoC designs. The Noxim simulator stands out among the many simulators that can be discovered in the literature. A lot of scholars use it since it supports wifi and is open-source. Hybrid wired-wireless networks aim to combine the finest aspects of the two strategies. In this study, investigation on various optimal configurations are carried out considering various test scenarios. Different parameters like Throughput, delivered packets, delay, and battery consumption and Packet Injection Rate are considered for optimisation. The findings demonstrate that the test cases utilised only require a small number of wireless routers, enhancing the metrics desired.

Keywords: Noxim, NOC, Network Throughput, Packet Injection Rate.

1 Introduction

The introduction of multiprocessor systems-on-chip was made feasible by the transistor's shrinking size (MP-SoCs). The bus becomes physically constrained when an MP-SoC connects many cores since this necessitates more communication between them. In response to this situation, Benini and De Micheli recommended using Networks-on-Chip (NoC) [1], which can make these communications more quickly and effectively. NoCs are a more effective option due to their scalability and ability for reuse. Networks-on-Chips are prepared by a group of linked routers that constitute a topology. Communication throughout the network is made possible by routers, which are in charge of transmitting messages from a source core to a destination core across the whole network. Because a router must offer a legitimate route to the packets aiming to decrease hops and a route with low latency, the distribution of the network graph directly influences how well data transmission works [2].

Wireless Networks-on-Chip (WiNoC) [3] are NoC topologies in which wireless routers are used for communication. Antennas on a wireless router exchange messages with other routers of the same kind to carry out all communication. By using this kind of communication, it is feasible to transmit packets between the topology's extreme points more rapidly, resulting in a reduction in latency under certain circumstances. However, there are significant drawbacks to this kind of communication in terms of the quantity of packets that are sent to the target router. A wireless structure may cause more packets to be dropped, which hinders the network's performance [4]. Investing in hybrid networks that combine traditional wired and wireless networks is one method to overcome this drawback. The measurements of average latency and packet loss may both be significantly improved with the usage of hybrid networks. The purpose of this kind of heterogeneous network is to counteract the drawbacks of each kind independently.

2 Previous works Done

Vincenzo Catania, et al, [5], proposed system was an open, scalable, and cycle-accurate network on chip simulator suggested system. In this study, we introduced Noxim, an open source, cycle-accurate platform for simulating both established wire-based NoCs and new WiNoC architectures.

Mostafa Haghi, et al, [6], proposed system was a new methodology in study of effective parameters in network-on-chip interconnection's (wire/wireless) performance. As a remarkable outcome, the

latency in a small network would increase by 71% if the subnet were expanded from 1 (wire network) to 16 (wireless network). As a result, it is always advised that the wireless connections paradigm be used in PIR-intensive environments.

Ivan Luiz Pedroso Pires, et al, [7], proposed system was trace-driven and processing time extensions for Noxim simulator. The Noxim extension that has been described will aid researchers in performance evaluations of fresh ideas using actual application traces. Work in the future will support wireless broadcast, virtual communication channels that help in stalemate avoidance.

Kun-Chih (Jimmy) Chen, et al, [8], proposed system was a NoC-based simulator for design and evaluation of deep neural networks (DNN). The results revealed that when compared to the conventional DNN design, the NoC-based DNN accelerator may cut off-chip memory accesses by 87% to 99%. Additionally, it was established that the neuron group size and NoC size are two essential design factors for maintaining good system performance in NoC-based DNN accelerators. Samuel da S. Oliveira, et al, [9], proposed system was Mapping Wired Links in a Hybrid Wired-Wireless network-on-Chip. The outcomes demonstrate that by using a heuristic method to alter the mapping of the links that connect the wireless routers to the wired routers, it is feasible to find wired-wireless networks that are more optimized for latency and delivered packets. We intend to replace hybrid mesh networks with erratic networks in upcoming research while simultaneously observing various traffic patterns and packet injection rates.

Simulation is one of the main tools used to analyse and test new proposals in the network-on-chip field. Several simulators can be found in the literature, among them the Noxim simulator stands out. It is being used by many researchers due to the wireless support and open-source availability. An important issue at the simulation phase is the choice of workload, as it may affect testing the system and its features. Although Noxim provides a simple support for input traces, it is very limited to a general behaviour of the system, accepting only a generic injection rate parameter over time. Another important part of the simulator is the ability to consider the Processing Elements processing time.

3 Tool Used

The current connectivity model used to construct all large-scale devices is known as Network-on-Chip (NoC). It is scalable, adaptable to many computational paradigms, and useful in a variety of contexts, such as high-performance multiprocessing machines. NoC communication is carried out via packets, which are broken down into tiny data units called flits, and sent from source to destination by routers, hubs, and network interfaces across wired or wireless lines. Simulation is a key technique for analysing traffic and measuring the performance, power, and area of NoC when designers wish to assess novel interconnection designs and organisations. It is a useful tool for evaluating the outcomes of novel thoughts and ideas without the need for hardware development. The simulator must adhere to cutting-edge recommendations and technology to ensure the correctness of the findings. Numerous specialised simulators for NoC interconnections are available now, including Noxim, Booksim, Naxim, Hornet, Topaz, HNOCS, NoC for OMNeT++, WNoC Simulator, Darsim, Netrace, Garnet, gpNoCsim, Nirgam, and NNSE. Gem5, CACTI, NS-3, and other simulators that aren't specifically designed for NoC might all be modified in some fashion. Only the specific-NoC simulator that was focused on performance and execution time and that was published in academic articles was taken into consideration in this work.

3.1 Noxim Configuration

The Noxim simulator supports a variety of configuration options, which may be categorised into the following classes: topology and structure, workload, dynamic behaviour, and simulations. Essential elements of the NoC, such as the total number of instantiated nodes and the kind of interaction between them, are included in the topology and structure class. Noxim divides nodes into tile nodes and hub nodes as its two classifications for nodes. The computing and storage nodes of the NoC are in the first group, while the second group consists of nodes that simulate a form of "gateway" for combining tiles and shortening distances between remote portions of the network. There are three distinct connectivity kinds that may be created: There are three types of connections:

- (a) Tile-Tile: It is a wired point to point connection which is in between tile nodes.
- (b) Tile-Hub: A tile and a hub element are connected via wire.
- (c) Hub-Hub: A linkage between two hub components. These connections can be both wired and wireless. The incorporation of wireless communication techniques in Hub-Hub interconnections, modelled using the idea of channel, considerably broadens the range of topologies supported by Noxim. The factors that govern how much and what sort of computation is sent to the NoC as input are all connected to the workload class. Each tile's activities are directly tied to these, and Noxim offers a number of widely used data traffic models that abstract standard communication patterns. Additionally, a genuine application's task communication graph may be mimicked by converting it into a unique table-based traffic. The dynamic behaviour-related parameters control how the NoC components make decisions during the simulation. These choices might be made in relation to packet routing between various network pathways, choosing between wireless and cable connection, etc. Although the Noxim Runtime Engine currently includes the most popular routing techniques, a key feature is the plugin-like design that makes it simple to test any new algorithm with minimum effort. The last group of parameters relates to the simulation setup, which may be modified to better meet requirements in terms of time budget (the amount of time available to run the simulation), quantity of necessary statistics, etc.

4 Methodology

4.1 Network Topology

The IP cores' physical configuration and how they are linked to one another via the network's connections are determined by network topology. There have been many various topologies proposed, including mesh, torus, binary tree, octagon, mixed, and bespoke topologies. The ease of physical construction, router complexity, and cable length make general purpose network topologies like rings and meshes ideal choices for on-chip networks. The most popular topology is 2D mesh because of its regular grid-like structure that is most suited for a chip's two-dimensional layout. Without changing the present node structure, it may be readily extended by adding new nodes and linkages. The ability of mesh to be divided into smaller meshes, which is a desired characteristic for parallel applications, is another factor in mesh's appeal. Several spatial topologies have been demonstrated in comparison studies to perform better than mesh and torus. They provide a unique network alignment technique in that solely relies on network topology architecture. In a mesh-based interconnect architecture called CLICHE was created by putting switches and computing resources in an m-by-n mesh.

4.2 Routing Algorithm

The routing method for a network topology determines the routes that packets between the source node and the destination node are sent over. Because the routing pathways would be unaware of the level of network congestion with oblivious routing, minimal latency and optimal throughput are not always possible. Non-minimal routing pathways may be used to balance latency and throughput in cases where the optimal throughput cannot be achieved with minimum routing. The routing patterns for adaptive routing algorithms can be adjusted to the current traffic conditions by avoiding the extremely congested lines. For monitoring and responding to network congestion, these adaptive routing algorithms need more complex control hardware. Here we are using One of the deterministic routing algorithms, Dimension-Ordered Routing (DOR), routes the packets first along one dimension and then along the subsequent dimension. This is why it is often referred to as the XY routing algorithm (first, X direction, then, Y direction). It is a well-known algorithm because of how easily and inexpensively it can be implemented because to its simplicity.

5 Experimental Setup

A systemC-based simulator named Noxim that is cycle accurate was used to evaluate wired NoC architecture. Mesh, butterfly, and baseline topologies were selected because of how well their inherent structures transfer to integrated circuits. These networks are also scalable and flexible using simple routing algorithms because of their physical regularity. Simulations are run under a variety of

traffic situations, including Butterfly, transposition, bit-reversal, and random, in order to determine how the architecture responds under various circumstances. There have been simulations at two network scales: 4x4 (8 nodes) and 8x8 (64 nodes).

Table 1. Simulation setup

Parameter	Description
Network Size	4x4,8x8
Network Topology	Mesh, Butterfly, Baseline
Packet Size	32
Wired Buffer Size	4
Number of Virtual Channels	1
Clock Cycle	1000
Routing Algorithm	XY, Odd_Even, DyAD,
Traffic Pattern	Traffic _Random, Transpose1, Butterfly, Shuffle.

6 Results and Analysis

The network throughput at which packet injection rate (PIR) starts to saturate is known as saturation throughput. It is a widely used statistic for assessing network performance. The rate of injection is 1 packet every 1000 cycles when PIR is set to 0.001. Since the size of the packets was set to 32 flits, the throughput was 0.0032 flits/node/cycle, or 0.001 packets/node/cycle.

Another crucial parameter for evaluating the effectiveness and calibre of a network connection is throughput. It can be expressed as flits/cycle and is defined as the network's capacity to handle the specified packet injection rate. Lower throughput and deteriorated performance will result from a high ratio of failure packet delivery. Several factors, including packet loss and network congestion, have an impact on the throughput of a network. Therefore, a network with a higher throughput will have a more efficient system. The figure 1 summarizes the comparisons of network throughput for Odd_Even routing algorithm in random traffic. The PIR of 0.4 has the highest network throughput.

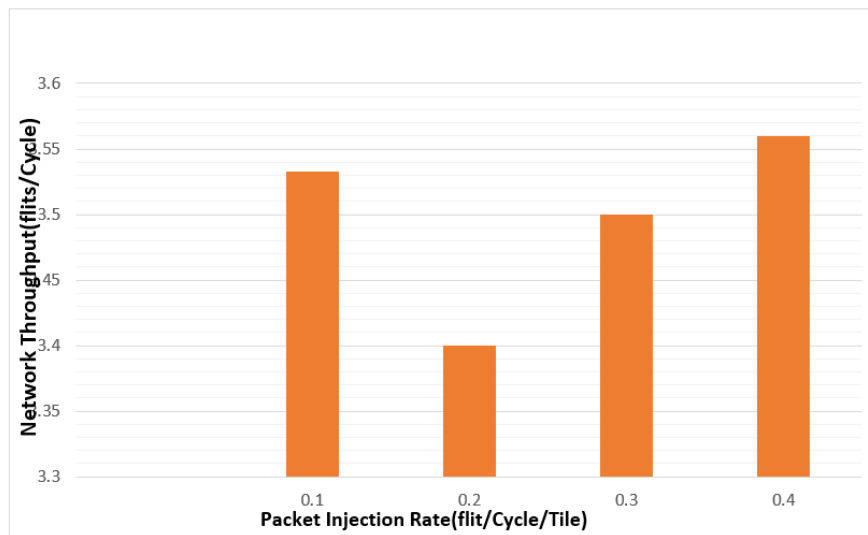


Fig 1. Comparison of Network Throughput for proposed Odd_Even Routing Algorithm in Random Traffic in 4x4 network size

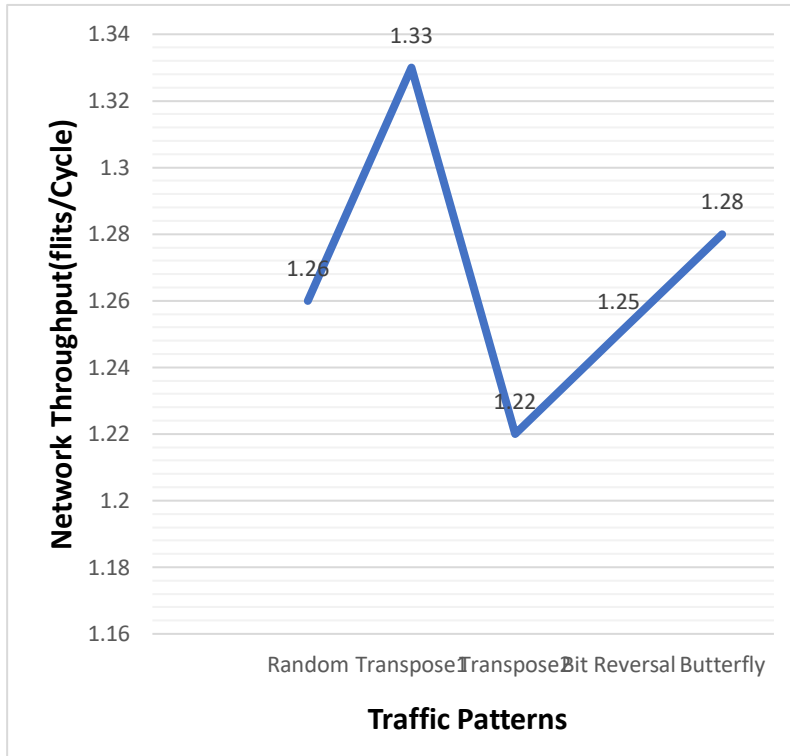
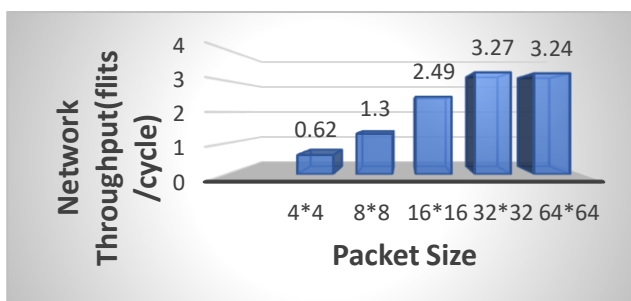


Figure 2. Comparison of Network Throughput of Odd Even Routing Algorithm for different Traffic patterns in 4x4 network size.

The probability of being injected every clock for each core is shown on the diagram's horizontal axis; the higher the injection rate, the greater the network stress. Each node in random traffic sends a packet to another node with a random probability. A uniform distribution of random numbers is used to decide the final destination of various packets. The figure compares network throughput of Odd_Even routing algorithm for different traffic patterns. The Transpose1 traffic pattern has the highest network throughput compared to other traffic patterns.

The figure 2 compares network throughput of Odd_Even routing algorithm for different traffic patterns. The transpose 1 traffic pattern has the highest network throughput compared to other traffic patterns



Five different network sizes—16, 64, 256, 4096, and 1024 nodes—have been simulated under random traffic distributions to examine the impact of network size. The results are shown in figure. Odd-even routing was chosen because it can handle greater network traffic. The network size 32x32 and 64x64

Figure 3. Comparison of Network Throughput have the highest network throughput. for different network size in Random Traffic in 4x4 network size.

Five different network sizes—16, 64, 256, 4096, and 1024 nodes—have been simulated under random traffic distributions to examine the impact of network size. The results are shown in figure 3. Odd-even routing was chosen because it can handle greater network traffic. The network size 32x32 and 64x64 have the highest network throughput.

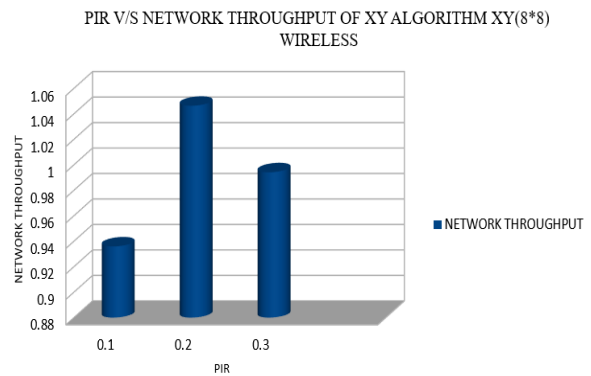
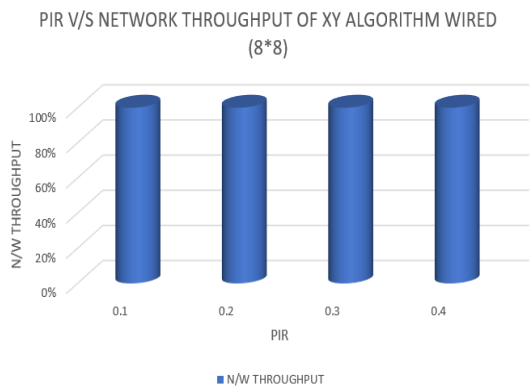


Fig 4. Comparison of PIR v/s Throughput of XY algorithm of wired network. (8*8) Fig 5. Comparison of PIR v/s Throughput of XY algorithm of wireless network. (8*8)

Comparison of PIR v/s Throughput of wired network. (8*8)

From The above graph Fig 4 we can see that, In Wired network with xy algorithm The network throughput remains constant in all four PIR value. Hence the highest throughput is achieved here. From The above graph Fig 5 we can see that, In Wireless network with xy algorithm The network throughput is increased in PIR value 0.2. Hence the throughput is less compared to the above wired network.

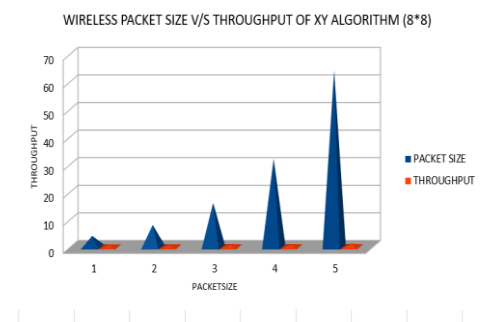
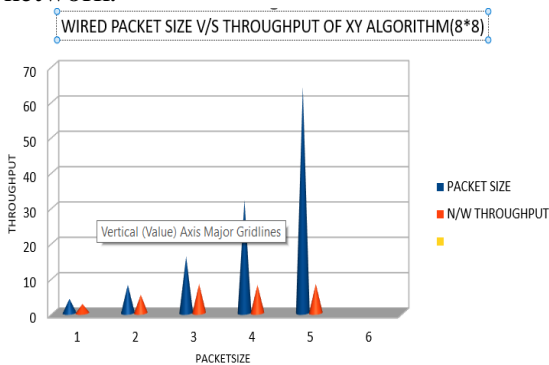


Fig 6. Comparison of packet size v/s Throughput of XY algorithm of wired network. (8*8)

Fig 7. Comparison of packet size v/s Throughput of XY algorithm of wireless network. (8*8)

From The above graph Fig 6 we can see that, In Wired network packet size with xy algorithm, The network throughput is very high in packet size of 5. Hence, we can see that as the packet size increases the network throughput increases.

From The above graph Fig 7 we can see that, In Wireless network of packet size with xy algorithm The network throughput is increasing as the packet size increases. Hence the by comparing wired and wireless, in both their will be increase in network throughput as the packet size increases.

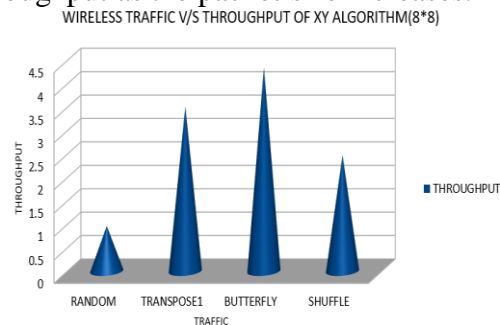
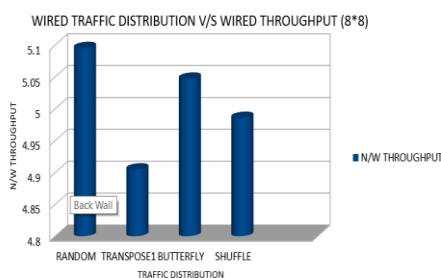


Fig 8. Comparison of Traffic Distribution v/s Throughput of XY algorithm of wired n network. (8*8)

Fig 9. Comparison of Traffic Distribution v/s Throughput of XY algorithm of wireless network. (8*8)

From The above graph Fig 8 we can see that, In Wired network with xy algorithm and different traffic distribution, The network throughput is high in random traffic distribution whereas less in transpose1. From The above graph Fig 9 we can see that, In Wireless network with xy algorithm and different traffic distribution, The network throughput is less in random traffic distribution whereas high in butterfly traffic distribution

Conclusion

Simulation is one of the main tools used to analyse new proposals in the Network-on-Chip field. Among all proposed simulators, the Noxim simulator stands out due to its accuracy near to a real system. In this paper, a wide range of simulations are conducted to compare the performances of three routing algorithms under a different traffic scenario with a network size of 4x4 and 8x8.

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