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# AI/ML/DL Algorithms and Applications in VLSI Design Technology Process Flow – A Brief Review

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**Abstract**

This paper gives a brief review of the AI/ML algorithms and applications that could be used in VLSI design technology. As the analysis and development of techniques that might lessen design complexity brought on by expanding process variability and shorten the turnaround time of chip manufacturing are clearly going to be a problem for the integrated circuit (IC) industry in the nanometre regime. The traditional approaches used for these activities are mostly manual, which takes time and resources. Contrarily, very large scale integration (VLSI) design and testing can take advantage of a variety of new automated ways thanks to the distinctive learning strategies of artificial intelligence (AI). Utilizing automated learning algorithms, AI and machine learning (ML) algorithms reduce the time and effort required to comprehend and process data within and across different abstraction levels, improving IC yield and speeding up production turnaround. This article examines the automated AI/ML methods for VLSI design and production that were previously used. The work presented in this paper is a technical seminar report of the P.G. (M.Tech) student, which is a part of the seminar that every student has to give w.r.t. any topic in the second semester of the PG programme.

**Keywords :** VLSI, Design, CMOS, Chip, Transistor

## 1. Introduction

In the world of microelectronics, CMOS technology has long dominated. On a single chip, the number of transistors manufactured has grown dramatically. The density and performance of these devices have increased due to the constant downscaling of transistors through many technical generations, which has greatly boosted the microelectronics industry's growth. Modern very-large-scale integration (VLSI) technology makes it possible to realise sophisticated digital systems on a single chip.

As transistor size go smaller, the complexity of the semiconductor manufacturing process rises. Simple scaling inevitably comes to an end as we get closer to atomic dimensions. Even these devices are small, several aspects of their performance decline over time, such as leakage increasing gain decreasing and increased sensitivity to manufacturing process fluctuations. The circuit functioning is severely impacted by the sharp increase in manufacturing differences, which results in inconsistent performance in transistors of the same size. This affects the circuit's propagation delay, which behaves as a stochastic random variable, making timing closure procedures more difficult and significantly lowering chip yield.

Affordable design at future technology nodes and advanced design techniques need to be adopted in the design flow for finer optimization in order to maintain the performance trend of VLSI systems handling the increasing challenges caused by increased process variability, design complexity, and chip integration. The effectiveness of electronic design automation (EDA) tools in overcoming design

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constraints determines how quickly a chip may be produced. The classic rule-based EDA approaches take a while to produce an ideal answer to the given design restrictions.
A number of issues have found noteworthy solutions thanks to artificial intelligence (AI). The foundation of AI is human intellect, which is understood in a way that makes it simple for machines to duplicate it and carry out tasks of various levels of complexity. AI is a subset of machine learning (ML). Learning, reasoning, predicting, and perceiving are the objectives of AI/ML. Large amounts of data may be quickly and simply analysed by AI/ML to find patterns and trends that help users make informed decisions. AI/ML algorithms are capable of processing multidimensional and multivariate data quickly. The fields of VLSI design and technology have seen substantial application of AI/ML techniques.

**2. Basics of VLSI Design Flow**

According to Fig.3.1, which depicts a generalised design flow that includes the front-end and back-end of full-custom/semi-custom designs, a traditional digital IC design flow contains numerous hierarchical layers. The functionality, interface, and overall architecture of the digital circuit to be built are all described abstractly in the design specifications. Block diagrams that include the functional description, timing requirements, propagation delays, necessary package type, and design restrictions are among them. They also serve as a contract between the vendor and design engineer.
The architectural design level determines the system's fundamental architecture, including the number of arithmetic logic units (ALUs), floating-point units, and processors with reduced instruction set computing (RISC) or complex instruction set computing (CISC). A micro architectural definition that includes the functional descriptions of subsystem components is the result of this level. A design's performance and power can be estimated by architects using these descriptions as a basis.
The next step is behavioural design; it gives a functional description of the design, frequently written in Verilog HDL or VHDL. The behavioural level hides the implementation specifics by providing a high level description of the functionality. The RTL level of description, which is the following level, is where the timing information is verified and checked.
A C/C++-based system specification can be automatically converted to HDL using a high-level synthesis (HLS) tool. The netlist, or gate-level description for the high-level behavioural description, is created by the logic synthesis tool. The time, area, and power requirements for the gate-level netlist are met by the logic synthesis tool. Testbench/simulation is used to carry out logic verification. At this point, formal verification and scan insertion using DFT (design for testability) are carried out to check the RTL mapping.
Floor layout, placement, and routing are done after system partitioning, which is the act of breaking large, complicated systems into smaller modules. The floor planner's primary job is to calculate the amount of chip space needed to implement a typical cell or module design. It also works to increase design performance. The submodules, gates, and flip-flops are placed via the place and route tool before the CTS and reset routing. The routing of each block is then carried out.
Layout verification is carried out after placement and routing to check whether the intended layout complies with the electrical/physical design guidelines and the source schematic. The chip enters the sign-off stage after the post-layout simulation, which involves the extraction and verification of parasitic resistance and capacitance. The finished product is transmitted to the semiconductor foundries for IC production as a GDS-II file.
Precision is essential for the numerous sophisticated and difficult physical and chemical processes involved in IC production. From wafer preparation to reliability testing, it includes many steps. In a nutshell, wafers are made by growing and slicing silicon crystals. The wafers must be polished to an exceptionally high degree in order for VLSI devices to have incredibly small dimensions. The deposition and diffusion of various materials on the wafer are two of the many processes in the fabrication process.

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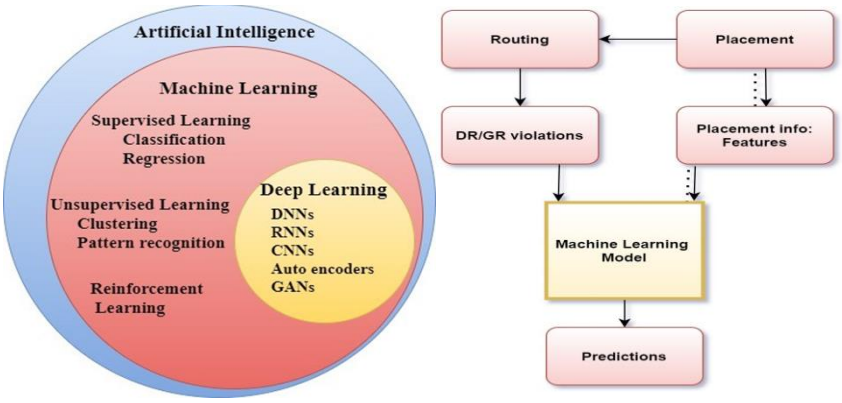


Fig. 1 : A view of the AI & ML algorithms flows represented diagrammatically

### 3. Note on AI & ML Algorithms

A machine may mimic human behaviour thanks to AI technology. The two primary AI subsets are machine learning and deep learning. With the aid of machine learning (ML), a computer may automatically learn from the data it has already collected. The most important subset of ML is deep learning (Fig. 4.1). As fresh data are added, ML includes learning and self-correction. Structured and semi-structured data can be handled by ML, whereas structured, semi-structured, and unstructured data can be handled by AI. The three main categories of ML are reinforcement learning, unsupervised learning, and supervised learning. Supervised learning occurs when the output label is present for each piece in the input data. Unsupervised learning is carried out when the only input variables are present in the data. Semi-supervised learning is the process of learning from data that has labels attached to some of the pieces.

### 4. Categories of AI ML DL

The two subcategories of supervised learning are regression and classification. Data analysis that uses classification derives models representing significant data classes. Classifiers are models that forecast discrete categorical class labels. Regression, as opposed to discrete class labels, is used to forecast missing or unavailable numerical data. A statistical method called regression analysis is frequently applied to the numerical prediction of continuously valued functions. Both numerical and class-label forecasts are referred to as "predictions" here. A learning function that predicts a mapping of Y = f (X), where Y is a collection of output variables for X input variables, can be seen in the classification/regression process. For estimating the related class label y of a given new tuple X, the mapping function is estimated. Support vector machines (SVMs), decision trees, random forests, ensemble learning, and linear, polynomial, and ridge regressions are examples of common regression and classification algorithms.

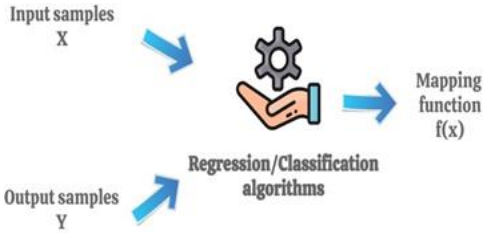


Fig. 2 : Learning function of classification/regression algorithms

### 5. Conclusive Remarks

A brief review of the VLSI design flow was presented in this paper. Deep learning, supervised/unsupervised/semi-supervised learning, NNs, MLP structures, and CNNs are a few examples of AI and ML approaches that offer chances to address the many issues and difficulties in the field of VLSI design. Artificial intelligence (AI) methods can lower the cost of testing a VLSI chip or subsystem. The design flow's various abstraction levels, from circuit design through chip

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production and testing, inevitably include a variety of models linking inputs to outputs. For instance, by applying AI heuristic search methods to locate an effective solution for rearranging the test cases, power consumption during testing can be decreased. On the chip, there are billions of integrated or future-integrated devices and components that exchange a huge quantity of data. With the help of AI/ML algorithms and the data gathered from various simulations and studies, it is possible to study the intricate I/O linkages between the components, processes, and different abstraction levels within each abstraction level. VLSI-CAD may make use of AI/ML solutions to optimise design flow. Future semiconductor difficulties may have ground-breaking answers provided by AI and ML.

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