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AnOverview on Advance Peripheral Bus design using System Verilog

Dhanush M[1],Dr. Sunil T.D[2], Dr. M. Z. Kurian[3]
[1]PG student, Dept. of ECE, Sri Siddhartha Institute of Technology, Tumkur,Karnataka, India.
[2]Associate professor, Dept. of ECE, Sri Siddhartha Institute of Technology, Tumkur,Karnataka, India.
[3]Head of the Department, Dept. of ECE, Sri Siddhartha Institute of Technology, Tumkur,Karnataka, India.

Abstract: APB's Design under test (DUT) is tested and it establishes connection between Test bench. It is designed based on reusable based methodology for SOC which is essential to meet the current APB constraint. This paper work involved is of APB protocol design and implementation here we are designing four test cases write transfer with and without wait, Read transfer with and without wait. The design is programed using Verilog and the concept of assertion is also involved in the design and the APB is verified using Synopsis tool.

Keywords: APB, Verilog HDL, Synopsis.

1. INTRODUCTION: APB belongs to AMBA-3 family. AMBA standards and specification are used for high level embedded microcontrollers design. AMBA protocol strongly support reuse peripheral devices to minimize silicon infrastructure. The APB is non-pipelined, used for low bandwidth peripheral. In order to simplify the integration of APB peripherals into a design flow every transaction is done at rising edge of clock. Each transaction take at least two clock cycle one for setup state and next for access state. APB is interfaced with AHB or AXI.

`1.1 APB block diagram:

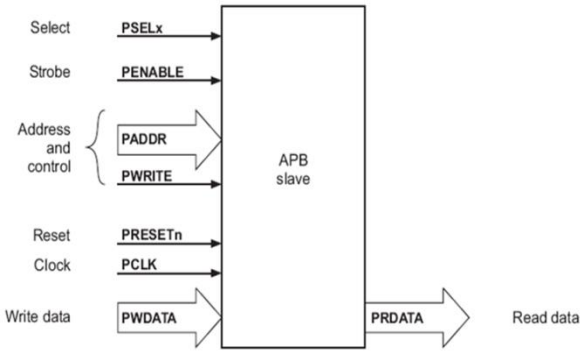

Figure 1 Block diagram of APB slave

1.2 APB signals:

s.no	Signal name	Signal function
1	PCLK & PRESET	APB works with rising edge of PCLK. PREST to reset APB.
2	PADDR	32 bit address, location mapping.
3	PSEL	Indication for Transaction start.
4	PWRITE	Direction signal. PWRITE=1: write transfer; PWRITE=0:readtransfer
5	PENABLE,PREADY	To indicate transaction incomplete.
6	PWDATA	Data is written in particular address.
7	PRDATA	Read data will appears when we call particular address.

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1.3 APB working model

APB working is modeled using Finite state machine. There are 3 states namely IDLE, SETUP and ACCESS states. In APB every transaction (read or write) takes at least 2 cycles. The APB FSM is shown in figure 2

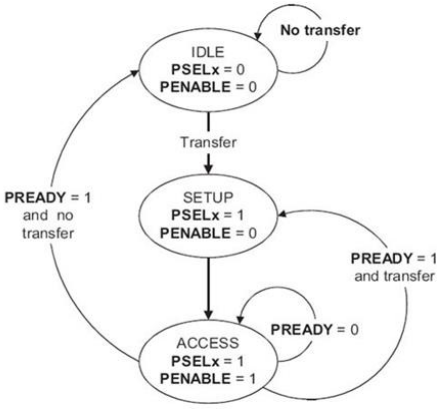

Figure 2 FSM of APB

Idle state-

- No operation performed.
- PSEL=0.
- PENABLE=0.

Setup state-

- APB enters to setup state when there is request for transaction.
- PSEL=1.
- PENABLE=0.

Access state-

- Indicate the start of transaction.
- All control and address signals are maintained constant.
- PSEL=1.
- PENABLE=1.

2. APB Write and Read Transfer

2.1 write transfer :

2.1.1 With no wait state

At T0,the bus stays at IDLE state. This is the default state for APB bus. For write transfer the bus is moves into SETUP phase, where appropriate select signal PSEL,PADDR, PWDATA and for write transfer PWRITE are asserted high at the rising edge of PCLK i.e., at T1.The bus remains in the SETUP phase only one clock cycle and then moves into ACCESS phase, i.e., at T2 the enable signal PENABLE and PREADY signal asserted high at the rising edge of PCLK. The write ,select, address, and write data signal and should be stable throughout the transfer complete at T3.The transfer is completed deasserted the PENABLE signal and PSEL signal also deasserted there is no more transfer to the same peripheral after completing the first transfer.

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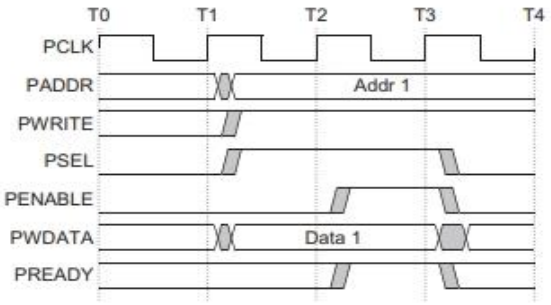

Figure 3 write transfer with no wait state

2.1.2 With wait state

PREADY signal makes to extend the transfer.first clock cyc le the bus is in the IDLE state.For the next rising edge of the clock the PSEL,PADDR,PWDATA and PWRITE signal asserted high.This is called SETUP phase.On the very next clock cycle it moves in to ACCESS phase at that time the enable signal asserted high,andwhene ever the slave ready to accept the transfer the slave asserted PREADY signal high.PADDR,PWDATA and all other control signal should be stable until the PREADY signal high.Bydeassserting the PREADY signal we can extend the transfer.

2.2 Read transfer :

2.2.1 With no wait state

At T0 the bus is in IDLE phase.For read transfer the PWRITE signal asserted low.InSETUP phase,at T1., the PADDR,PSEL are asserted high and PWRITE signal deasserted low at the rising edge of PCLK.Thenxt rising edge of PCLK the enable signal PENABLE and ready signal PREADY asserted high to make a transfer this phase is called ACCESS phase.All signal remains stable throughout the read transfer.PRDATA signal used to read the data before the read transfer.

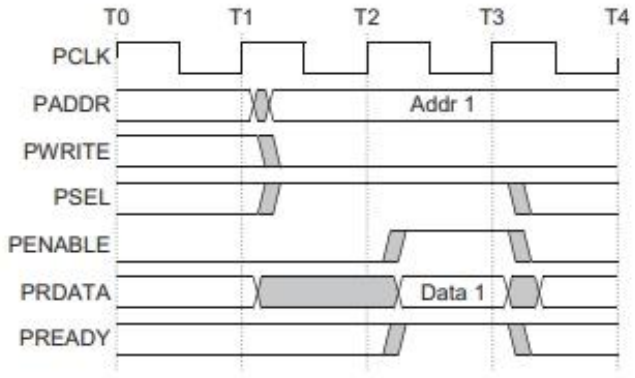

Figure 4 read transfer with no wait state

2.2.2 With wait state

The IDLE phase and SETUP phase are remains same as read transfer with no wait.In ACCESS phase the PENABLE asserted high but the PREADY signal is asserted low.This indicates that the salve is not ready to accept the transfer and also we can extened the read transfer by making the PREADY signal low.when the PREADY signal is asserted high then the slave is ready for read transfer.All signals remains unchanged throughout the transfer.

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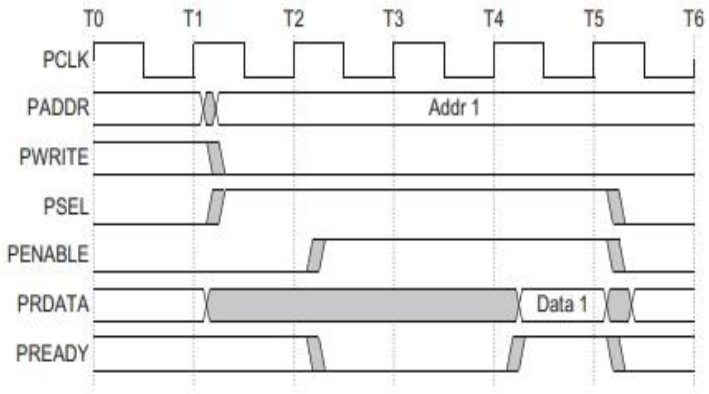

Figure 5 read transfer with wait state

3. Assertion: assertion is basically the statement of truth made about the design by design or verification engineer. The engineer will assert that several condition are always true or never true for the design. If that claim is never been proven, then assertion fails. System Verilog assertion are built from sequences and properties, an assertion works by continuesly attempting to evaluate sequence or property.

4. Conclusion : This paper gives an overview design of APB protocol transaction and operating model for APB, the craiteria to be considerd for design.

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