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Trends in Design of Low Power Circuits Using Level Shifting Buffers for Multi Supply Systems

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***Abstract*— Power and performance efficiencies are the most important design parameters in system – on - chip design. Numbers of methods were developed for reducing the power and delay by reducing supply voltage and multi supply voltages. Multiple supply voltage designs need voltage level conversions between multiple voltage domains. This is achieved by the application of voltage level shifter (LS) circuits. LSs are an interfacing circuit which interconnects low core voltage to high core voltage and vice versa. LS ease communication among diverse modules. However literature reported that the conventional LSs suffer from delay variation due to dissimilar current driving transistors along with high power dissipation. This paper presents the identification of limitations and design aspects of existing LSs through an extensive literature survey and to project the current state of LSs. This study concentrates on multiple supply voltages, power consumption, and speed of processing in ICs. The detailed literature review is expected to pave way for addressing the issues and challenges related to LSs and helps in design and development of efficient low-power multi-voltage LSs in the design aspects of VLSI circuits.**

Keywords **— Multi VDD systems, Power consumption, Delay, Level Shifter, IoT, Su-threshold voltage.**

I. INTRODUCTION

The scaling in size and addition of more functional densities on digital Integrated Circuits (ICs) have given ascends to large power consumption per unit area. Power consumption of IC is one of the prominent design constraints out of speed and area. Power consumptions in VLSI are includes static, dynamic and leakage power consumption. The dynamic power consumption is a resultant of switching of load capacitance when different voltages and dependent of frequency of operation [1]. The static power is because of direct short circuit path between VDD and ground. Leakage power is due to leakage current arise from substrate-injection and sub-threshold regimes, hence enough attention can be laid on leakage power reduction. The Power consumption at system level can be reduced by scaling power supply voltage, but the problems like voltage swing, leakage currents, and insufficient noise margins would start to originate with the supply voltage scaling and speed or delay depends on circuit topology. In view of portable and handheld devices the power consumption has turn into most significant design constraint for VLSI designers as the frequency or charging of battery back. The increase in power consumption and reliability problem also rises in addition to packaging cost. The best approach is usage of multi-VDD systems and multi VDD module are interfaced by Level shifters (LSs) and the leakage power depends on total number of MOS transistors and their operating point in spite of the switching activity [2]. LFSR counter analysis using CMOS sub-micrometer, so as to attain smaller chip size with lofty operating speeds and efficient usage of energy. From the results it is clear that the LFSR counter has additional benefits when compared to other counter parts, therefore it is a new trend setter in the field of communication for computing applications [3]. In the field of communication, energy efficient computing will play a vital role to maximize the circuit performance when we operate the device at sub threshold or near threshold regime. The effective solution to minimize the energy consumption of a circuit is MTCMOS at low power applications and GLBB is at ultra low power applications [4-5]. The results show that the proposed design achieves very good performance in terms of power and delay. The change detection and background removal application can be also realized by division operation. In image analysis, if only integer division is performed, then the results are typically rounded at the output to the next lowest integer [5].

II. STATE OF ART LEVEL SHIFTERS

A. Differential Cascaded Voltage-Switch Logics LSs

A new low-power level shifter (LS) is provided for effective voltage shifting from near/sub-threshold to above-threshold sector. The new architecture brings together the multi threshold CMOS method along with novel

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topological variations to assure an considerable voltage transformation, with limited energy and static power consumption. The design has implemented in 90nm technology, the proposed circuit reliably converts 0.18V input signals to 1V output signal, while maintaining signal frequency of 1 MHz, also process voltage temperature variations are considered. The Post layout simulations results demonstrates that the new LS have low propagation delay, static power dissipation, and lower energy per transition at an input voltage 0.2-V, 1 MHz pulse [6].

A conventional topology on voltage level shifter (VLS) for its power and delay parameters poses a special feature called built in short circuit protection, increases the speed, and reduction in power consumption is depicted in fig. 1. Unlike the available conventional LSs, the proposed VLS not requires complex digital timing signals. The VLS design was designed in CMOS 180nm process technology. The speed, power consumption of the VLS is compared with the best bench mark designs. The proposed VLS outperforms in both speed and power consumptions than the available designs. Simulation results have performed at layout extraction level and validated the design robustness [7-10].

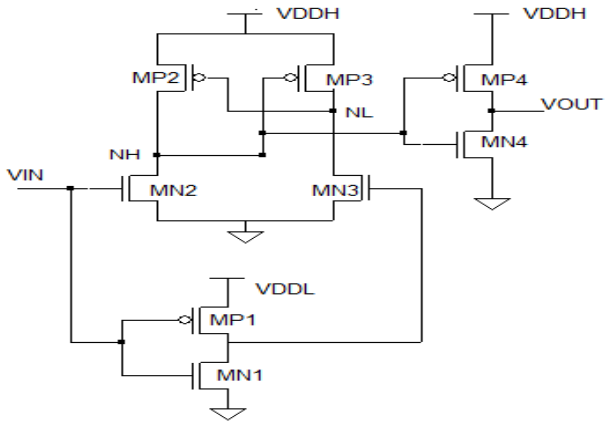

Figure 1. Differential Cascaded Voltage-Switched Logic Level Shifters

The LS circuit described about importance of dual supply voltage design by a clustered voltage scaling (CVS) design is an efficient approach to decrease chip level power consumption. The most advantageous CVS design relies on LS implemented in a flip flop to reduce energy, delay, and area penalty due to level shifting. Moreover, circuit robustness besides supply bounce is a important property that differentiate good LS design. Two new level shifting flip-flops incorporate with half-latch type and a precharged type. These flip flops are characterized in the power delay design space to attain 30% reduction of power delay product and around 10% savings in total power of a CVS design as compared with the conventional flip flop. The projected flip flop also show 18% layout area decrease. Advantages of Level shifting in flip flop in contrast with asynchronous level shifting are important parameters to be considered are delay penalty and its sensitivity to power supply bounce [11].

B. Contention Mitigated Level Shifter

The design is suitable for system level Dynamic Voltage & Frequency Scaling (DVFS) environment or multiple power domain circuit blocks. In order to attain low power and high performance in IC consisting of circuit blocks having different supply voltages, the proposed design utilizes the circuit techniques for achieving less capacitive loadings signals and to reduce the contention between pull up to pull down network through positive feedback. The design performs both level up and level down shifts and are designed to perform on wide range of voltages from 0.6V to 1.6V. The new technique improve the delay and signal distortions and slew rate of signals, for verification with existing designs, the simulation is carried out at 0.13 μm and 0.35 μm CMOS technologies. The results show that the delay and signal distortions are improved over available LSs [8], [12].

Circuit describe about importance of LS in the realization of low cost passive Radio Frequency Identification (RFID) tag, fabricated the system in a bulk CMOS process without additional process steps. RFID system memory utilizes non-volatile memory array with bit cell, consumes ultralow-power depicted in fig. 2. Cell requires the application of a 10V potential between the cell control line for program and erase operations. In this pair of voltage driver networks have introduced, that utilize novel methods to overcome these challenges. In addition, the analysis of dynamic behavior of standard level shifters has studied. This analysis has applied to GIDL free level shifters to attain optimized area, speed performance, and lower power consumption by provide a sizing methodology. The LS drivers were designed and fabricated by TowerJazz 180nm bulk CMOS process technology [22-30].

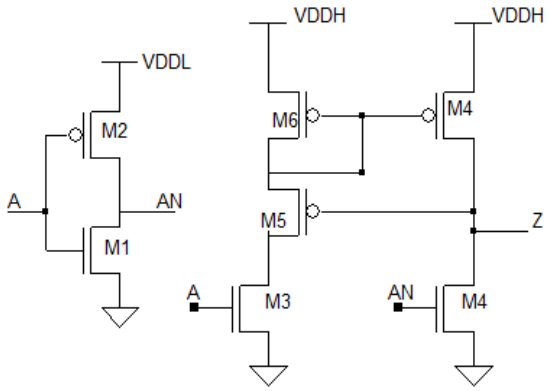

Figure 2. Contention Mitigated Level Shifter

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C. Pass Transistor Level Shifter

The Pass transistor LS have reduced the impact of normal and reverse temperature dependences on very low voltage LSs. The speed, delay, and power consumptions and variation tradeoffs on two LS designs are examined for a wide range of voltage swings. The circuit drives strengths and Process voltage Temperature corners are analyzed by using commerciality available technology tools. The developed Pass Gate level shifter is found to be better power and delay performance than the conventional DCVSL level shifter, however, limited operating range makes DCVSL is superior then pass gate type of LS [12-16].

D. Multi- Vth Level Shifter

The circuit developed has low-power single supply level shifter for thin oxide film transistor [16]. The developed LS circuit suitable for performing level conversion from 10V to 20V without any logic circuit, by using n-channel oxide thin film transistors. The results showed that, the level shifter operates correctly with oxide thin film transistors and the active power consumption is as low as 0.2mw at the signal frequency of 10 KHz.

Multi threshold voltage LSs are suitable for low voltage applications to change from sub-threshold to above threshold domain. They developed circuit which mixes the multi threshold CMOS methods and novel topological modifications, to guarantee wide-voltage translation range with low static power and energy consumptions. They have justified their designed work with mathematical values [17-28].

E. Transmission Gate Level Shifting Buffer

Transmission gate is the basic circuit element used in the transmission gate LS designs. Its ON resistance is less than the ON resistance of the NMOS, as ON resistance is low the lower transition times results in the output which reduces the delay and avoids contention mitigation [22]. Transmission gate LS reduces the Dynamic and leakage power consumptions, depicted in fig. 3.

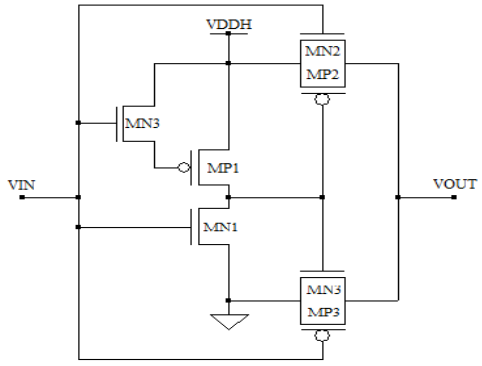

Figure 3. Transmission Gate Level Shifting Buffer

The LS operates well below sub threshold regimes. The minimum input level of the LSs is 160mV. In Fig. 4, the output node voltage (VOUT) of the Transmission Gate Level Shifting buffer is 1V. The output voltage of the LS achieves a higher value, and its slew-rate is not affected. As the output node of TG Level shifting buffer resulting in less current being supplied to the output node. A higher output value of buffer and improved output slew-rate provides the dynamic-energy efficiency and performance benefit due to current in the circuit does not need to pass for a longer time and there is no contention as well.

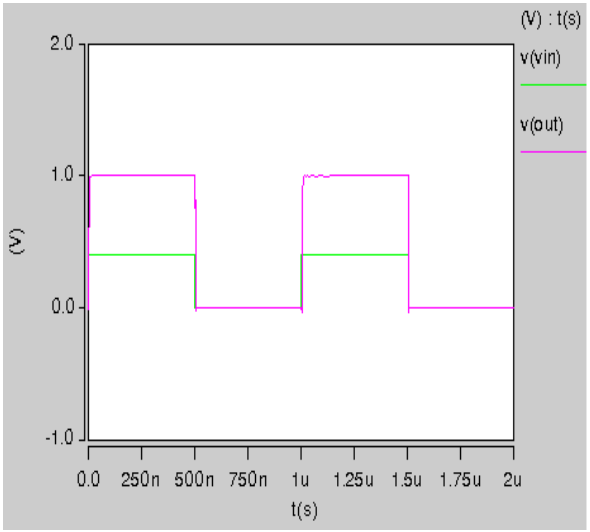

Figure 4. Level up shift of Transmission Gate Level Shifters

III. COMPARATIVE ANALYSIS

Model Simulation results of the LSs for different types of topologies are depicted in table I. It can be observed that the circuit designed with TG [22] has low power consumption even at higher VDDL and its active power of 19nW at 90nm technology compare with other level shifter at the same technology [19-21]. The maximum operating frequency of the circuit is at 100 MHz also produced stable output depicted in fig. 4. The minimum values of VDDL for which the circuit operates correctly at 1 GHz are 0.11V.

Table I Comparative analysis of state art LSs

Work/Ref.	Tech. (nm)	VDDL (V)	VDDH (V)	Active Power (nW)	Delay (ns)
[18]	65	0.16	1.1	73	22.6
[19]	90	0.18	1.2	91	10.7
[20]	90	0.14	1.2	45	15.8
[21]	90	0.20	3.0	151	10.4
[22]	90	0.23	1.4	19	2.06

IV. CONCLUSION

In this brief, state of art voltage level-shifting buffer architectures was reviewed, which are able to convert very low-input voltages to above threshold voltage. The efficiency of transmission gate voltage level shifting circuit is dominating the other buffers, due to the fact that the current of pull-up device is drastically reduced while pull-down device is drastically pulling down the output node voltage, but the strength of the pull-down circuit is also drastically increased. Simulation results are strongly supporting in terms of power and performance metrics. The transmission gate voltage level shifting circuit compared with other w**O**rks, especially from the power consumption viewpoint.

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