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Leakage Reduction Methodology in CMOS for the Design of 1-Bit Full Adder

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***Abstract*— This paper presents low leakage and high speed 1-bit full adder projected with low threshold NMOS transistors in associations with universal logic gates which leads to have reduced power and delay. The customized NAND and NOR gates, a necessary blocks, are presented to design a proposed adder cell. The simulations for the designed circuits performed in cadence virtuoso tool with 65 nm CMOS technology at a supply voltage of 1 Volts. The proposed universal gates and 1-bit adder cell is compared with conventional NAND/NOR gates and 1-bit adder. The proposed adder schemes with modified universal logic gates achieve significant saving in terms of delay which are more than 24% and which is at the cost of 5% when compared with conventional designs.**

Key words—Leakage Power, universal gates, 1-bit Full Adder, CMOS, Delay

I. Introduction

With improvements in technology and the growth of mobile applications, energy efficiency [1] and power consumption [2] has turn into a significant focus in VLSI digital circuit design. Recently, digital sub threshold circuit design has turned out to be a very promising method for ultralow power applications [3-4]. The adder is one of the most critical mechanisms of a processor, as it is used in the arithmetic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access [5-6]. A dominant component of power consumption in today's VLSI circuits is leakage power when to operate the circuit in ultra sub threshold region [7].

The CMOS Current limiters are accompanying in practical electronic circuits to supply the current limit for different loads with the provision of preventing the design to generate and transmit higher current levels for unsafe effects due to any short circuit or no load. The double level current limiters are more predominant to achieve low power consumption with nanosecond delays [8]. The "Built in Self Test (BIST)" is a most suitable application in sub system design for its counter and decreasing error analysis using CMOS nanometer, so as to attain lesser chip size with snooty operating speeds and efficient usage of energy. Therefore, it is a new trend setter in the field of testing the design before to tape out IC for computing applications by employing more than one logic style, means hybrid logic style [9-10].

MTCMOS technology may perhaps a solution to accomplish the low power and high performance design necessities of modern designs [11]. It provides the designer with transistors that are normal, fast (with a high leakage) or slow (with a low leakage). MTCMOS makes use of both low as well as high threshold transistors and hence is an effective circuit technique that paves a way for low power and high performance design [12].

The intuition is to design a 1-bit full adder to attain noteworthy reduction in leakage current. The benefits of standard CMOS style-based adders/subtractors with 28/40 transistors are its robustness against voltage scaling and transistor sizing; while the shortcomings are high input capacitance and requirement of buffers [13-14]. The multiple-V_{th}, multiple-V_{DD}, and transistor size, are useful to decrease the power in digital circuits [15-17], have described about variation of supply voltage level to each operation to decrease the average power consumption. In their presentation a framework on evaluating the above parameters and effectiveness of each of these approaches independently.

The designs offered by Basha et al. (2013), Gundala et al. (2015), Sanapala and Sakthivel (2017) and Mohanthy (2019) outlined the computing systems for energy efficient methodologies for low voltage applications. From the conducted literature survey it has been observed that the maximum research was carried out based on 1-bit full adder. The paper is organized as follows: Section 2 describes the procedure of proposed methodology by using universal logic gates. Section 3provides the result and analysis. Finally, section 4 provides the conclusion for this paper.

II. PROPOSED METHODOLOGY

In this methodology, two NMOS transistors in series with low threshold voltage (V_{th}) form a parallel combination with one capacitor is connected between the bottom of pull down network and ground terminal of conventional CMOS NAND and NOR gate as shown in figure 1.

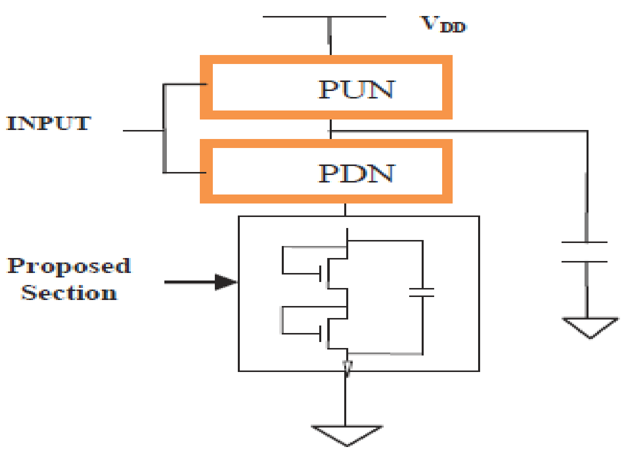

Fig.1. Block diagram of proposed methodology

The leakage current is lesser, if two transistors are connected in series, which enhances the stacking effect. This inspires us to connect two NMOS transistors in series. An extra capacitor is injected in between the pull down network and GND in parallel with the two series transistors. This capacitor blocks large portion of static leakage current flow. This is conceivable due to the high reactance of a capacitor to zero frequency signals. The schematic diagrams for the proposed NAND and NOR gates with the above methodology is shown in the figures 2 and 3 respectively. The simulated waveforms for the proposed universal gates after post layout simulations are shown in figure 4 and 5 respectively.

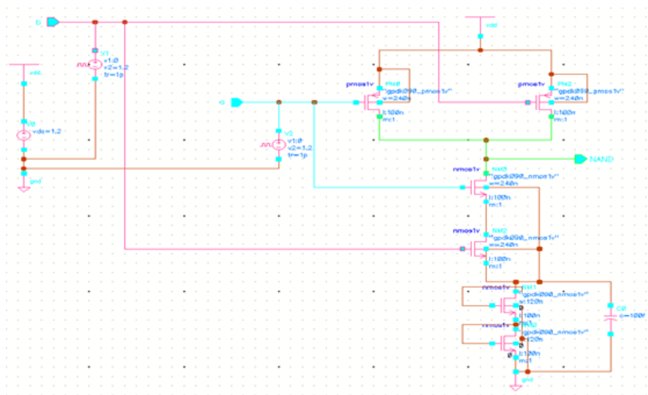

Fig.2. Circuit diagram of Proposed NAND gate

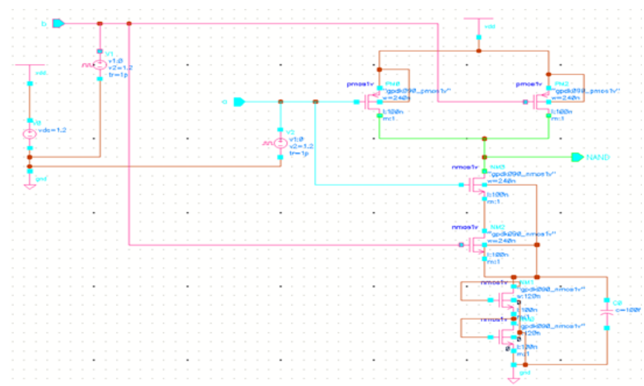

Fig.3. Circuit diagram of Proposed NOR gate

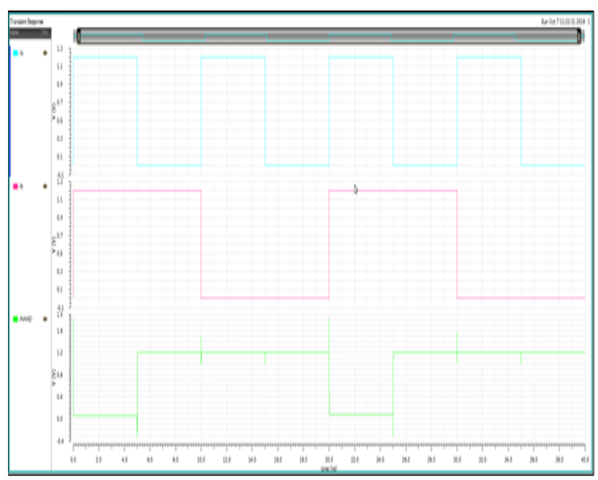

Fig.4.Post layout waveform of Proposed NAND gate

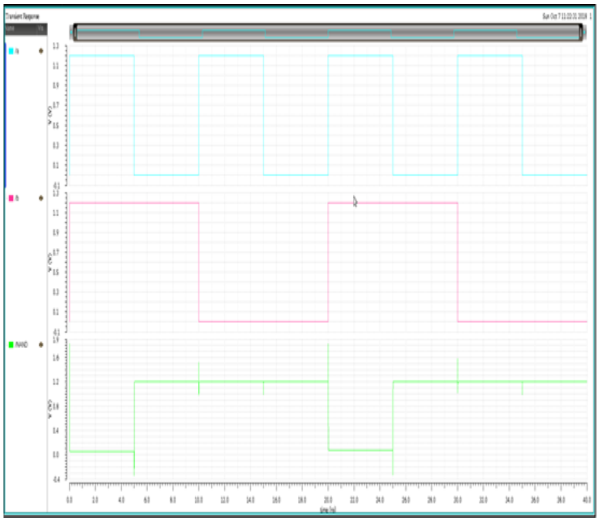

Fig.5.Post layout waveform of Proposed NOR gate

In this work, the above concept is extended to design a 1-bit full adder circuit. Formerly, the study has been carried out to design the conventional adder structure by dividing it into four blocks. The Conventional 1-bit adder structure is shown in figure 6. The four different parts of adder circuit which is shown in above figure, could be divided into one or several blocks by adding proposed section as shown in below figure 7. On the other hand, when large numbers of external blocks are added, and then delay time drops and power consumption rises for the same goal. The circuit diagram and post layout waveform of proposed one bit full adder were shown in figures 8 and 9 respectively.

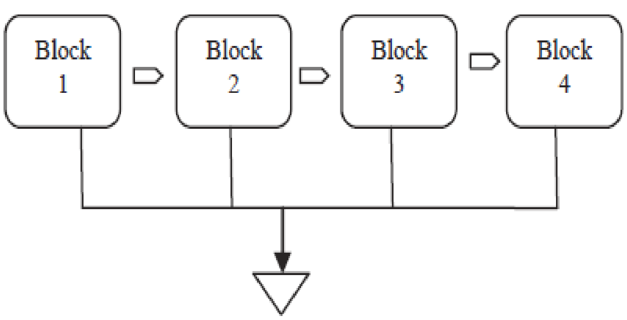

Fig.6. Block diagram of Conventional Adder

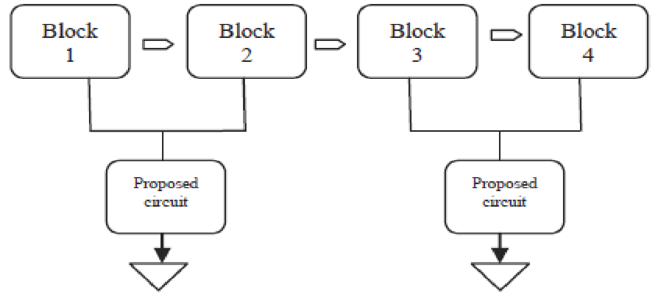

Fig.7. Proposed approach for one bit full adder design

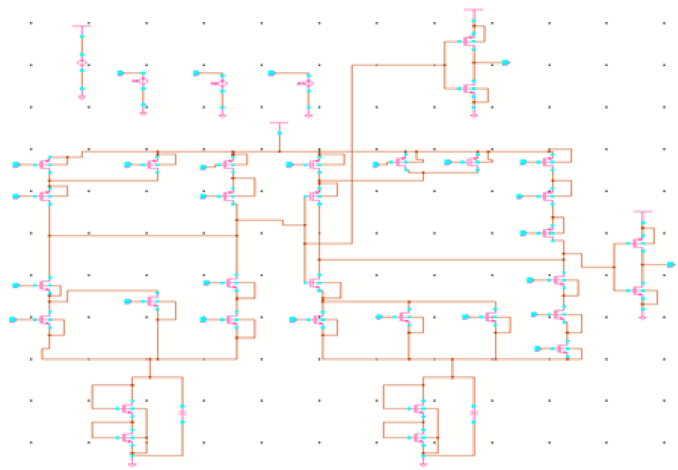

Fig.8. Circuit diagram of proposed 1-bit full adder

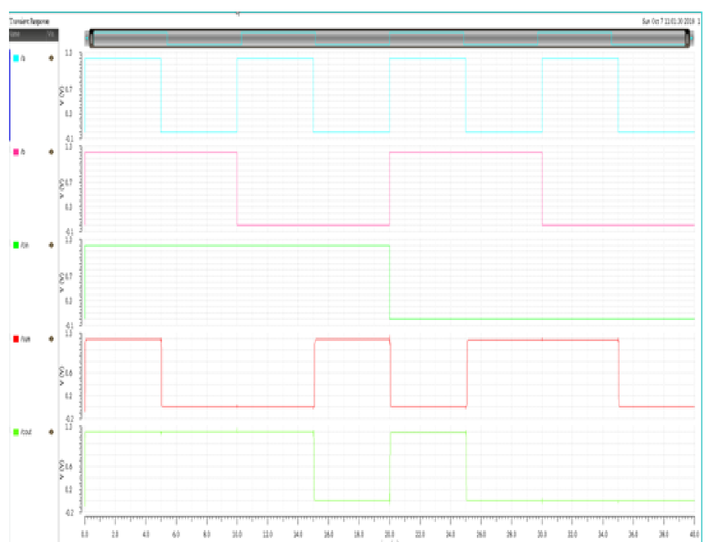

Fig.9. Post layout simulation of proposed 1-bit full adder

III. RESULT AND DISCUSSION

Table I. Simulation of conventional and proposed universal gates

Design	Leakage Power (nW)	Delay (pS)
NOR	0.13	13.1
Proposed NOR	0.091	11.9
NAND	1.059	9.5
Proposed NAND	0.762	8.73

Table II. Simulation of conventional and proposed adder circuit

Design	Average Power(uW)	Delay (ns)
Conventional adder	1.306	0.1192
Proposed adder	1.43	0.09

The simulation of conventional and proposed NAND/NOR gates and one bit full adder is shown in table I and II respectively. The simulations for the proposed full adder circuits are performed in cadence virtuoso tool with 65 nm CMOS technologies at a supply voltage of 1 Volts. The proposed NAND gate achieves significant saving in terms of delay which is more than 7% and average power is more than 28% when compared to basic NAND gate. Similarly, the proposed NOR gate achieves significant saving in terms of delay which is more than 9% and average power is more than 30% when compared to basic NOR gate . Though, the proposed adder cell is better in terms of leakage power consumption and lower delay, but at the cost average power consumption.

IV. CONCLUSIONS

In this paper, l-bit full adder is presented which is employed by proposed NAND and NOR gates. All the simulations are carried out on cadence tool by using 65 nm technologies to estimate the proposed design and existing designs. From the results it has been observed that the design has lowest delay and minimum leakage power when compared to conventional adder circuits. The proposed adder schemes with modified NAND/NOR gates achieve noteworthy saving in terms of delay which is 24.5% when compared with conventional "C-CMOS" 1-bit full adder.

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