Low Power and Area Efficient 4-2 Compressor for Signal Processing Applications

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Abstract—**In this paper, two performance metrics power and delay are estimated for various XOR-XNOR circuits and Multiplexer for designing 4-2 compressor. The main objective is to design an energy efficient compressor for computing applications in FIR filter. The simulations for the designed circuits performed in cadence virtuoso tool with 45 nm CMOS technology at a supply voltage of 0.9 Volts. The proposed 4-2 compressors consist of six blocks out of which two XOR-XNOR blocks and four MUX blocks. The average power, delay and energy consumed by the proposed compressor which is based on 5T XOR-XNOR and GDIMUX design is 85.72 nW, 62.53 pS and 5.36 aJ respectively.**

Keywords: XOR-XNOR module, MUX, GDI, 4-2 Compressor, Delay and Energy.

I. INTRODUCTION

In a microprocessor or a digital signal processor (DSP), data path plays a prominent role since performance metrics like the die-area, speed of operation, power dissipation etc., depend directly on the efficiency of data-path [1]. In computer arithmetic and high performance system, such as FIR filters, the multipliers and dividers are the most important part. In most cases, the multiplier consists of three stages. The second stage (i.e. reduction of partial products) is most important stage.

This stage is only accountable for the power and delay. So as to accumulate partial products, compressors are used at this stage to reduce the partial products and critical path [2-3]. Power and delay are the two performance metrics which comprehensively decide the energy metric of the system in low power application and high performance computing in IoT applications. [4-5].

Leakage power dissipation is eventually becoming comparable to dynamic power dissipation in many high performance designs when the design is at near threshold computing applications. The very large level of integration results in complication of heat removal; this in turn increases the cost of cooling and packaging [6].

In this paper, various XOR-XNOR gates with reduced transistors are proposed to design an energy efficient 4-2 Compressor for computing applications. The rest of the paper is organized as follows: Section 2 describes literature survey and proposed circuit implementation is introduced in section 3. Section 4 presents the result and discussion. Section 5 draws the conclusion.

II. LITERATURE REVIEW

G. Venkata Rao et. al., proposed [7] a

dynamic comparator with low power, high speed and low offset voltage has been proposed in order to make the ADC efficient. Design is based on pre amplifier re- generation circuit and a latch. The result of the proposed design shows that the circuits are more optimized in terms of delay, power consumption, and power delay product at the cost of reduced voltage swing.

The Level shifters are assembling circuits. To assemble "Multiple functional circuit blocks" multiple LSs are required, commonly for "Low voltage to high voltage translation" LSs are employed and "High to voltage to low translation" inverters are adequate at the cost of additional circuitry [8]. The author presented a "Novel high performance Dynamic Voltage Level Shifter" to act as assembling circuit between multiple functional circuit blocks. The result reveals static power of 4.6 Nano Watts.

Circuit Power consumption, area and delay are the majority important design issues being addressed by many algorithms. Among different types of Delay and power reduction techniques "Clustered voltage scaling" techniques is the best way, it patricians the design into multiple voltage blocks, "High speed sensitive voltage blocks" are biased with higher VDD to increase the speed performance and "Low speed sensitive voltage blocks" may be biased with lower VDD to decrease power consumption [9-10].

Multi voltage clustered structures are the fundamental and imperative power lowering techniques; utilize voltage Level shifter (LS) circuits to intercommunicate "Multiple voltage circuit blocks" to shrink power at core or circuit modules. The LS may deem as delay and power expenditure when its individual contributions are high. The developed Diode current limiter LS have implemented in 130nm technology, which minimizes power and delay at the cost of area overhead [11].

Optimization at the logic level can be achieved by minimizing the logic by its equivalent and Boolean based logic reduction, logic level power down alike. Logic level power down controls the logic switching activity at the expense of additional circuits. Optimization depends on the circuit complexity and other factors at this level. Upto 50% power consumption can be possible with these methods. Pass transistor based MOS Switch Integrated Ultra Low Power 1-bit full adder (MOSSI-ULP) is the design by Vijaya kumar and Reeba Korah for which the biasing techniques are applied to restore the full swing [12].

Y. Amar Babu et al., proposed [13] a novel area and power efficient on chip communication architectures for image encryption and decryption using single soft processor (Micro Blaze). Proposed System On Chip explores On chip Communication architectures features to efficiently implement the application. The SoC offers scalability and guarantees on the timing behaviour when communicating data between various processing and storage elements. Proposed SoC has been implemented on Spartan6 FPGA and evaluated at 83.33 MHz. It has occupied only 19% of resources available on target FPGA, consumes very low power 68 mW, 15% of conventional architectures. The proposed on chip communication architectures compared with device utilization on FPGA and power consumed.

Various energy efficient arithmetic circuits at low supply voltages and ultra-low supply voltages have been proposed by various authors namely adder, multipliers, subtractor, divider and level shifter in the literature [14-18].

From the literature it has been clear that power and delay are the two performance metrics which can decide the energy metric of a digital circuit in low power applications.

III. PROPOSED METHOD

Compressor is extensively employed in realization of multipliers to reduce the partial products. The 4-2 compressor has five inputs and three outputs and which is shown in below figure 1.The five inputs are compressed into three outputs, where X1, X2, X3, X4, Cin are the inputs and Cout, Carry, Sum are the outputs.

Here output Sum and input X1, X2, X3, X4 has same weight. The proposed 4-2 compressors consist of six blocks out of which two XOR-XNOR blocks and four MUX blocks which are shown in figure 2.
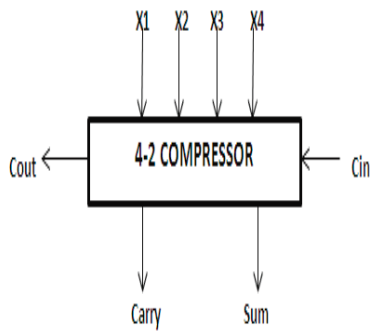
The circuit diagram of CMOS 5T XOR-XNOR module, GDIMUX and proposed 4-2 compressor were shown in figures3, 4and 5 respectively. Figure 6 shows the post lay out waveform of proposed 4-2 Compressor.
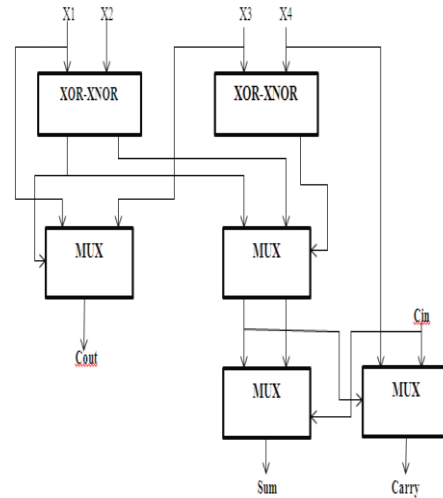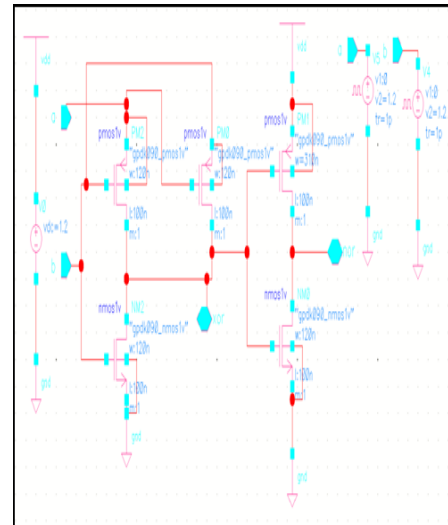

Fig.2. Logical decomposition of 4-2 compressor
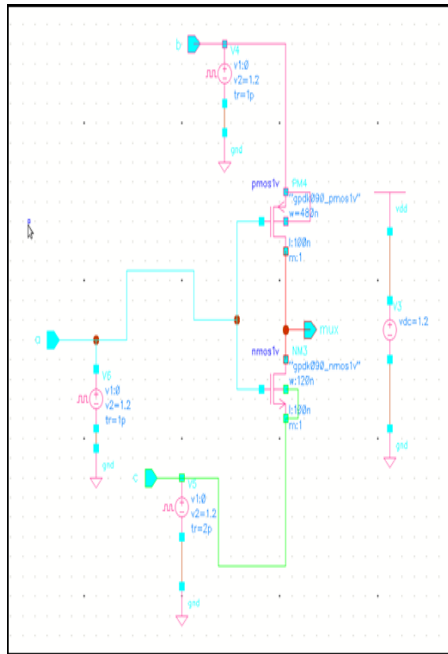

Fig.3.Circuit diagram of 5T XOR-XNOR

Fig.1. Compressor block diagram

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Fig.4.Circuit diagram of GDI MUX
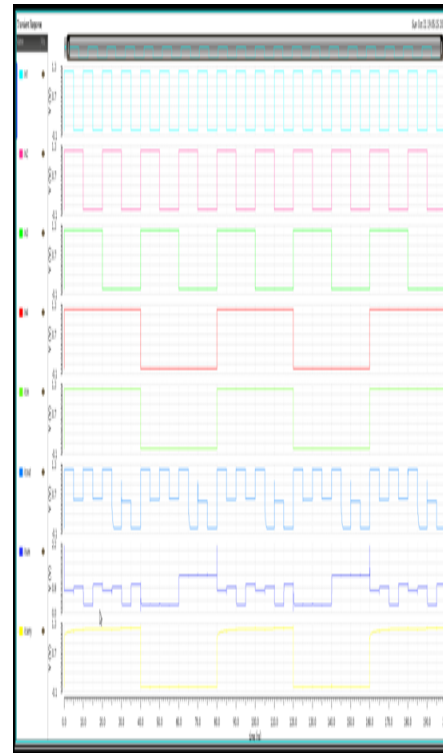
Fig.5.Circuit diagram of proposed 4-2 Compressor

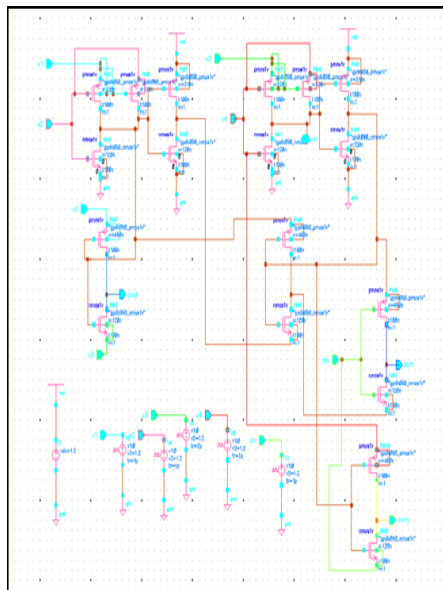**Fig.6.Post lay out waveform of proposed 4-2 Compressor**

IV. RESULTS AND DISCUSSION

Initially the conventional CMOS XOR-XNOR gate and MUX logic is simulated at 45nm technology as they are the basic block for any digital systems, then the simulation has been carried out for proposed 4-2 compressor which employs 5T XOR-XNOR gate and GDIMUX logic. Based on the three different XOR-XNOR gates and Mux a 4-2 compressor was proposed.

The simulation results of proposed design along with conventional and existing were shown in table 1. From the results it has been clear that the propagation delay and energy for the proposed design is less both in case of

5T XOR-XNOR gate as well as GDIMUX gate at cost of average power consumption.

Performance metrics of Proposed 4-2 compressor was depicted in figure 7.

TABLE 1.
SIMULATION RESULTS OF VARIOUS CIRCUITS

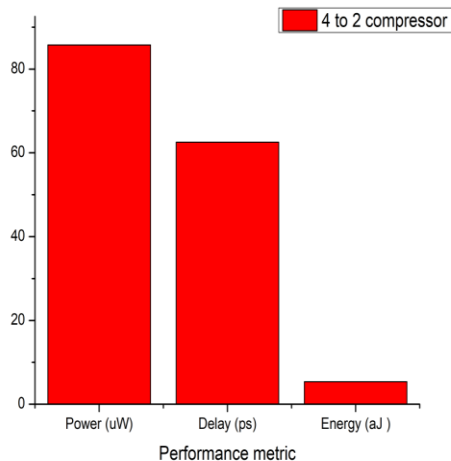| Design	Average Total Power (nW)	Delay (ps)	Energy (aJ)
CMOS XOR-XNOR	827.6	42.1	34.841
8T XOR-XNOR	805.2	29.5	23.753
5T XOR-XNOR	2800	4.5	12.6
CMOS MUX	661.7	42	27.791
TG MUX	393.8	12.1	4.764
GDI MUX	981.9	3.1	3.043
Proposed 4-2 compressor	85.72	62.53	5.36

Fig.7. Performance metrics of Proposed 4-2 compressor

V. CONCLUSIONS

In this work, an energy efficient 4-2compressor was designed. The simulations for the existing and the proposed circuits have been carried out by using Cadence Tool at 45nm technology.

The proposed design was analyzed with the existing CMOS and 8T XOR-XNOR based compressors. The design is energy efficient with 5TXOR-XNOR module and GDIMUX unit based 4-2 compressor. The average power, delay and energy consumed by the proposed compressor which is based on 5T XOR-XNOR and GDIMUX design is 85.72 nW, 62.53 pS and 5.36 aJ respectively.

The proposed designs perform better than the existing ones in terms of power, delay and power-delay product (energy).

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