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Energy Efficient GDI Based Full Adders For Computing Applications

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***Abstract*— This This paper presents energy efficient GDI based 1-bit full adder cells with low power consumption and lesser delay with full swing modified basic logic gates to have reduced Power Delay Product (PDP). The various full adders are effectively realized by means of full swing OR, AND and XOR gates with the noteworthy enhancement in their performance. The simulations for the designed circuits performed in cadence virtuoso tool with 45-nm CMOS technologies at a supply voltage of 1 Volts. The proposed 1-bit adder cells are compared with various basic adders based on speed, power consumption and energy (PDP). The proposed adder schemes with full swing basic cells achieve significant savings in terms of delay and energy consumption and which are more than 41% and 32% respectively in comparison to conventional "C-CMOS" 1-bit full adder and other existing adders.**

***Keywords*— VLSI, high speed, energy efficient, GDI full adder. .**

I. INTRODUCTION

The demand and reputation of handy electronics is motivating designers to strive for lesser silicon area, lower delays, longer battery life, and more consistency. For any system, power consumption can be reduced by scaling the supply voltage and operating frequency. Whereas, it increases the propagation delay of the circuit and which in turn degrade the driving capability of the entire design [1-2]. In recent days a novel low power hybrid adders have introduced for on-chip communications, which works with smaller amount of energy for its operation. In the field of communication, energy efficient computing will play a vital role to maximize the circuit performance when we operate the device at sub threshold or near threshold regime [3-4]. This paper proposes an innovative "low-power" design technique that allows solving the majority of the trouble mentioned above - Gate Diffusion Input (GDI) technique [5]. The GDI move towards for implementation of a broad range of complex logic functions using only "two transistors". The rest of the paper is organized as follows: Section 2 describes literature survey and proposed circuit implementation is introduced in section 3. Section 4 presents the result and discussion. Section 5 draws the conclusion.

II. LITERATURE REVIEW

The power expenditure is a most important concern for emerging appliance like smart phones, smart cameras, multimedia processors, etc. The power expenditure can diminish by number of approaches. The "Multiple Supply Voltage" (MSV) design is a prevailing technique for the diminution of power consumption of System on Chips (SoCs). The SoCs uses Voltage Level Shifters (VLSs) and the VLSs would become overhead while its own power expenditure & circuit delay is high. The VLSs become efficient with feedback network to remain the output voltage stable at all possible loading conditions. Robustness of the VLSs can be examined at high frequencies with standard unit of loads with elevated temperature. The VLS are the key interfacing components in all most all SoCs in recent days [6-8].

The CMOS Current limiters are more practical electronic circuits having a provision of current limit for different loads with the provision of preventing the design to generate and transmit higher current levels for unsafe effects due to any short circuit or no load.

The most common current-limiters are realized to have a voltage drop from too high to low voltage supply rails. In practical cases, where the power rail voltages need the in-house current-limiters, they are habitually built using current sensors, current control circuits and pass transistors. The double level current limiters are more predominant to achieve low power consumption with nanosecond delays [7].

Ebrahim Pakniya et.al. [8] proposed a design "energy efficient 16T FA cell for near-threshold voltage

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technology". This paper focused about two new structures of one - bit full adder circuits suitable for sub-threshold voltage. Comparison has been carried out for propagation delays, power dissipations, PDP, and EDP in sub threshold regime.

GDI logic scheme [10] is introduced as a substitute to C-CMOS logic. It is a low power design method which offers the execution of the logic function with less numbers of transistors. GDI gates offer abridged voltage swing at their outputs, i.e. the output low (or high) voltage is deviated from the ground (or VDD) by threshold voltage Vth. The decrease in voltage swing is advantageous to power consumption. Alternatively, this may guide to time-consuming in the case of cascaded operation. Due to this degraded output, the circuit may leads to malfunction, at low VDD operation. As a result, particular concentration must be essential to attain full swing operation.

To decrease the overall "power consumption" and "propagation delay" a new full adder scheme is designed with full swing basic GDI cells. This logic cell employed with OR/AND and XOR gates. The sum and output carry is chosen without the help of inverters. Proposed design has full output swing and is found suitable when operated at lower voltages to maximize the energy efficiency.

III. PROPOSED METHODS

The standard GDI cell is shown in Fig.1. Even if it resembles like a conventional CMOS "C-CMOS" inverter, the source/drain diffusion input of together PMOS and NMOS transistor is dissimilar.

In basic inverter circuit, source and drain diffusion input of PMOS and NMOS transistors are for all time tied at VDD and GND potential, correspondingly. In contrast, the diffusion terminal acts as an external input in the GDI cell. Various Boolean functions can be realized with the help of GDI cell such as AND, OR, INVERTER, MUX, F1 and F2, as listed in Table 1.

In this section, various full adder designs by featuring GDI cell with full logic swing are proposed with an objective to decrease the circuit complexity and to attain higher speed at cascaded operation.

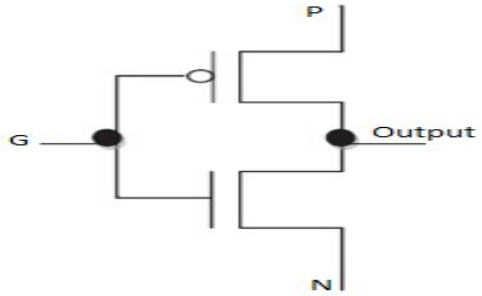

Fig.1. Standard GDI cell

TABLE 1. VARIOUS BOOLEAN FUNCTION REALIZATIONS USING GDI CELL

N	P	G	Output	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

The approach is to keep away from threshold voltage losses by means of full swing gates. So as to achieve full swing output, a new XOR gate is proposed and its performance is compared with the existing circuits. Three GDI full adders were designed based on the proposed full swing XOR gates and their performances are also compared with other adders found in the literature in terms of speed of operation, power consumption and energy. The circuit diagram of GDI based XOR gate is shown in figure 2

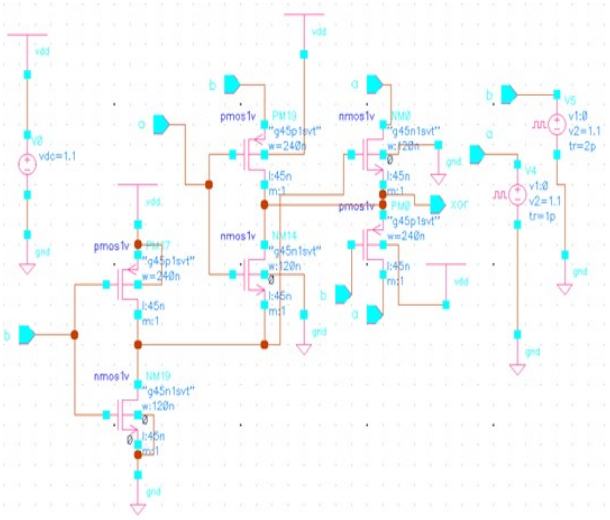

Fig.2. Circuit diagram of GDI based XOR gate

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The design of GDI full adder with full swing can be achievable with the help of full swing gates such as AND, OR and XOR discussed in the preceding part. This design totally avoids the swing restoration buffers that results in enhancement in the performance. Three possible full swing GDI full adders are designed by rewriting the full adder design expression with the help of three basic gates And, OR and XOR to accommodate the full swing gates. The circuit diagram of proposed "GDI Full Adder" based on design 1 and 2 shown in figures 3 and 4 respectively. The post layout simulation waveforms of full swing XOR circuit and proposed GDI full adder circuits are shown in figures 5, 6 and 7 respectively

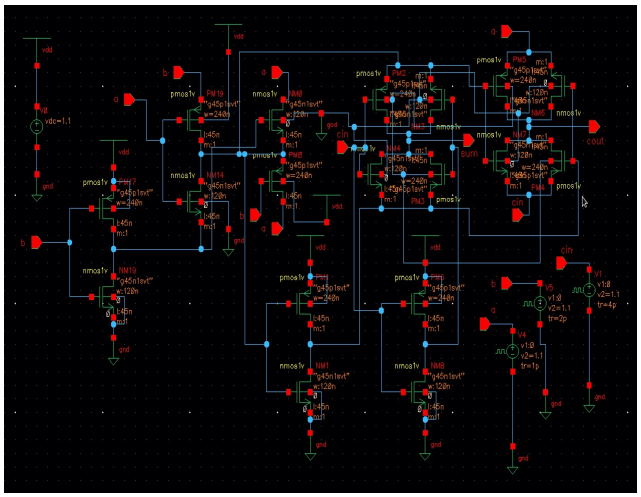

Fig.3. Circuit diagram of proposed GDI full adder (Design 1)

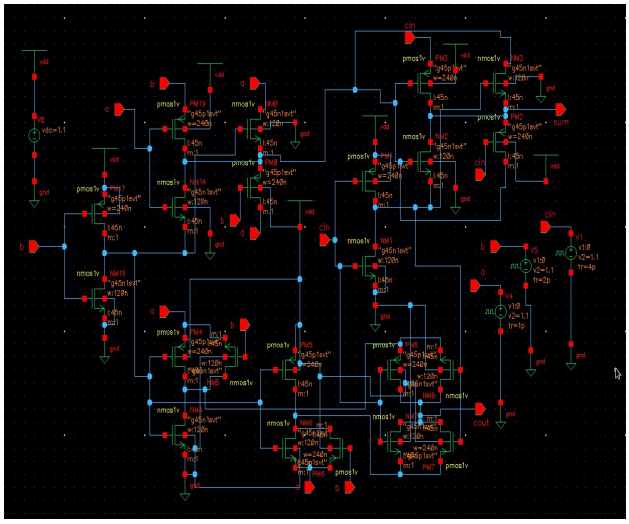

Fig.4. Circuit diagram of proposed GDI full adder (Design 2)

Fig.5. Post layout wave form of XOR circuit

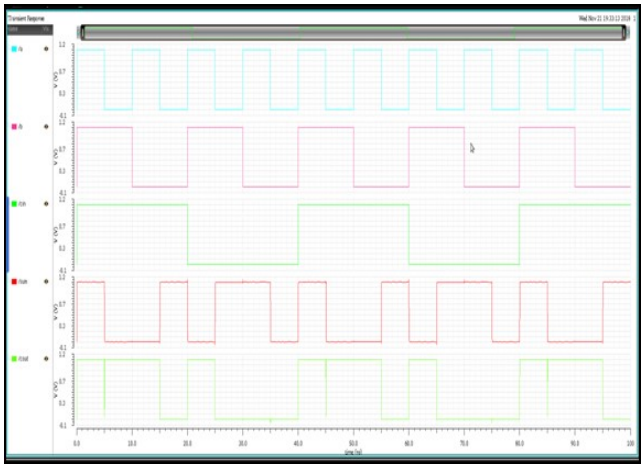

Fig.6. Post layout wave form of proposed GDI full adder (Design 1)

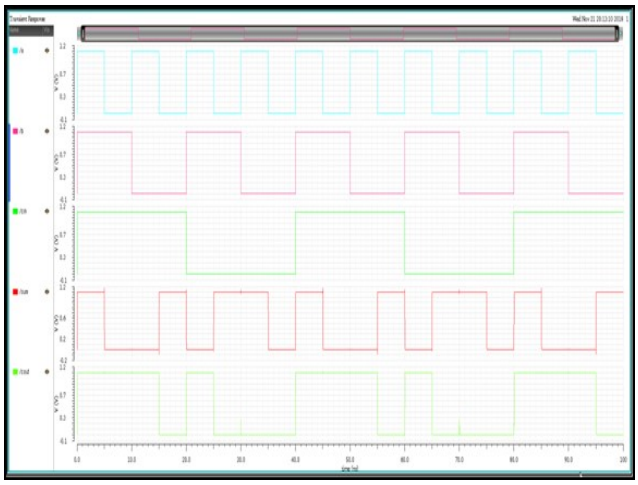

Fig.6. Post layout wave form of proposed GDI full adder (Design 2)

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IV. RESULTS AND DISCUSSION

Simulation results of different XOR gates at 1 Volts are shown in Table 2. The graphical analysis of existing and proposed XOR gates in terms of delay, power and PDP are depicted in figure 7. The simulations for the proposed GDI full adder circuits are performed in cadence virtuoso tool with 45-nm CMOS technologies at a supply voltage of 1 Volts. The proposed XOR gate achieves more than 67% delay, 48% power consumption and energy (PDP) of 83% as compared to C- CMOS and other counter parts. Similarly, the simulation results of different full adder designs are shown in Table 2. From the results it is clear that the proposed design-2 which is based on full swing XOR gate function is better in terms of power, delay and energy consumption as compared to C-CMOS and existing GDI based adders from the literature.

TABLE2. SIMULATION RESULTS OF VARIOUS XOR GATES

Design	Power (nW)	Delay (ps)	Energy (aJ)
CMOS	547.3	23.2	12.6
Existing 1	403.1	22	8.8
Existing 2	396.2	21.1	8.3
Existing 3	381.8	20.2	7.7
Proposed XOR	280.8	7.6	2.1

TABLE3. SIMULATION RESULTS OF VARIOUS FULL ADDER DESIGNS

FA Design	Power(uW)	Delay (ps)	Energy (aJ)
CMOS	0.975	46.2	45.1
Existing 1	1.31	41.3	54.1
Existing 1	1.685	49.13	82.7
Existing 1	1.462	32.2	47.1
Design-1	0.927	37.8	35.1
Design-2	1.14	26.8	30.6

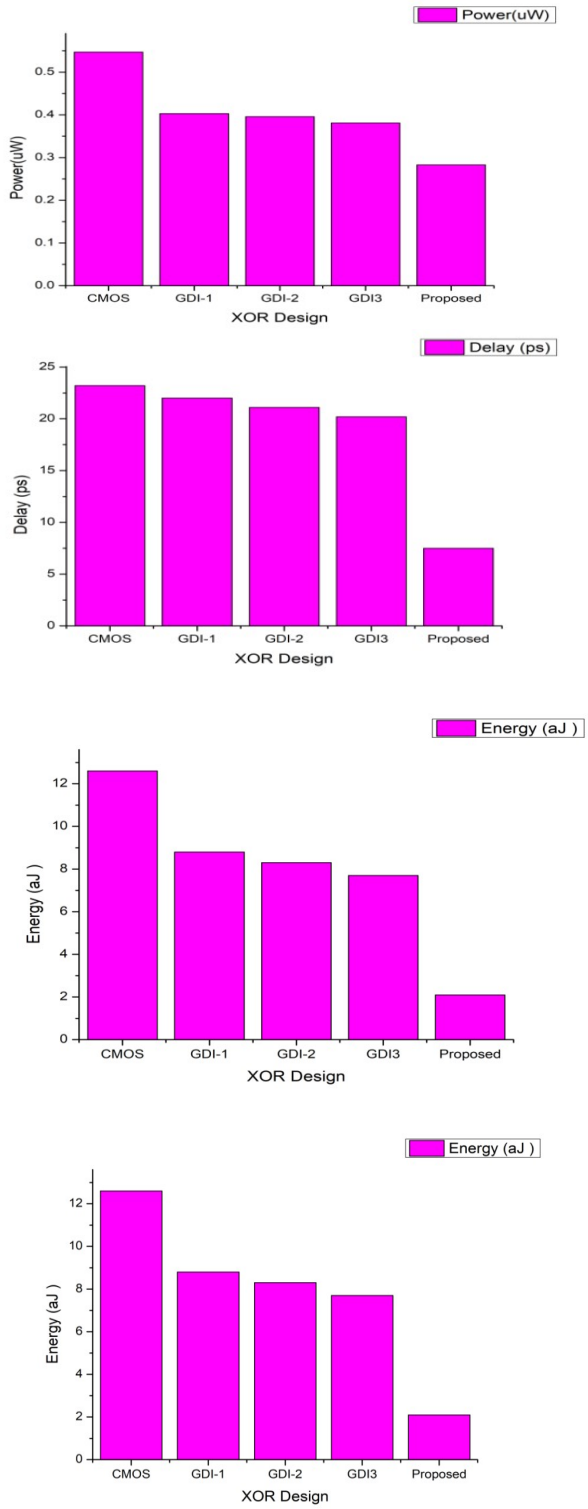

Fig.7. Performance metrics of different XOR designs at 1 Volts

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V. CONCLUSION

In this paper, GDI based l-bit full adder circuit is presented depends on energy efficient full swing modified logic gates. All the simulations are carried out on cadence tool by using 45-nm technologies to estimate the proposed design and existing designs.

From the results it has been observed that the design has lowest delay and minimum PDP when compared to numerous existing adder circuits. Subsequently, the proposed GDI full adder is set up suitable choice at low operating voltages with full swing output. The proposed adder schemes with full swing logic gates achieve significant savings in terms of delay and energy consumption and which are more than 41% and 32% respectively when compared with conventional "C-CMOS" 1-bit full adder and other counter parts. From the performance point of view, it clear that, the design might be a choice in the upcoming SoC applications

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